Precise Implementation of CDTA

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Abstract. *The Current Differencing Transconductance Amplifier (CDTA) is a popular active building block for analog signal processing. Since it is not available as a commercial IC, most of the CDTA applications are verified only via simulations or the CDTA is implemented by commercial circuits. The paper deals with CDTA implementation, emphasizing the accuracy, linearity, and dynamic range of the processed signals, and low power consumption. Such a CDTA can be useful wherever these requirements are more relevant than the speed and bandwidth, typically for implementing hardware emulators of memristive systems.*

Keywords

Accuracy, CDTA, CDU, dynamic range, implementation, OTA.

1. Introduction

The Current Differencing Transconductance Amplifier (CDTA) introduced in 2003 [1] or its simplified versions Current Follower Transconductance Amplifier (CFTA) [2] and Current Inverting Transconductance Amplifier (CITA) [3] have become popular building blocks for designing various linear and nonlinear analog circuits, particularly frequency filters [4], oscillators [5], wave generators [6], triggers [7], and accurate rectifiers [8].

Since the CDTA is not currently available as an off-the-shelf device, most of the proposed CDTA applications are checked only via simulations, using models of both classical CMOS [8] or bipolar [9] structures and also low-voltage low-power techniques [10]. In most cases, however, the end stage is a design and compilation of the corresponding SPICE code. The only exception known to the authors of this text is an experimental chip, designed and manufactured in 2007 in the 0.7 µm CMOS technology [11], which does not comply with today's demands for low power consumption and linear offset free characteristics of the internal blocks of the Current Differencing Unit (CDU) and Operational Transconductance Amplifier (OTA).

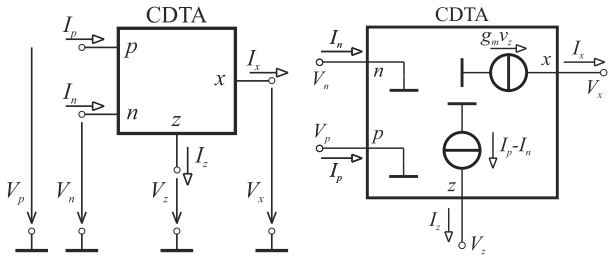
Less commonly, with the aim of completing the simulations with experimental verification, the CDTA is built from other off-the-shelf ICs. Then the CDU can be implemented via two Positive Current Conveyors of the 2nd Generation (CCII+) [12], which are part of the transimpedance OpAmp AD844. The popular LM13700 or similar circuits can be used as the subsequent OTA stage. The so-called diamond transistor OPA860 is used in several designs [13]. However, in all the above cases, the linear operation of the CDTA can be accomplished only within a narrow dynamic range. On the other hand, it is desirable to extend this region towards the limits given by DC supply rails. As regards the OTA, the only commercial type, MAX435(436) with a generic linear voltage-to-current characteristic, is not currently available. Moreover, none of the above ICs is a low-power, low-offset, or high-accuracy device.

The paper summarizes some results of designing the CDTA, consisting of the accurate CDU and OTA with rail-to-rail linear DC characteristics, and operating in a frequency region of up to hundreds of kHz. Since the CDU is also designed on the basis of OTA, the linear OTA, or voltage-controlled current source, is the core of this modular concept.

2. CDTA

The basic version of the CDTA with schematic diagram as in Fig. 1(a) is a block with four terminals. The p and n low-impedance terminals serve as inputs for currents I_p and I_n. The high-impedance z terminal generates a current I_z equal to the difference between the I_p and I_n currents, and the high-impedance x terminal is internally interconnected with the z terminal via the OTA stage with the transconductance g_m. The corre-

sponding behavioral model of the CDTA is shown in Fig. 1(b). Since the input part of the CDTA, providing the I_z current as a difference between input currents, is called Current Differencing Unit (CDU), the CDTA can be considered an interconnection of the CDU and OTA.



(a) Schematic symbol. (b) Behavioral model.

Fig. 1: CDTA.

CDTA as an ideal functional block can therefore be modeled by a set of equations:

$$\begin{pmatrix} V_p \\ V_n \\ I_z \\ I_x \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & g_m & 0 \end{pmatrix} \cdot \begin{pmatrix} I_p \\ I_n \\ V_z \\ V_x \end{pmatrix}. \qquad (1)$$

Note that, for the sake of increasing the CDTA universality, the number of its current x terminals can be increased, and the directions of the corresponding currents I_x can be modified. On the other hand, the CDTA layout can be simplified for applications where one of the p or n terminals is not utilized. Such single-input CDTAs are then denoted as CFTA (Current Follower Transconductance Amplifier - with only the p terminal) [2] and CITA (Current Inverter Transconductance Amplifier - with only the n terminal) [3]. Another known modification of the CDTA is the ZC-CDTA (Z-Copy CDTA). Details are given in [3].

3. CDTA Implementation

The proposed conception of the CDTA implementation is shown in Fig. 2. The currents I_p and I_n are sensed by two fixed resistors R. The difference between their voltage drops is transformed to the output current of the OTA with the transconductance $g_m = 1/R$, and the current flowing out of the z terminal is equal to the difference between the currents I_p and I_z. If the R value is chosen low enough (up to 100 Ω), then these resistors directly determine the low-input resistances of p and n terminals. Such a design starts from the fact that, particularly for CMOS implementations of the CDTA, these resistances can be even in kΩ values [5] and, in addition, they are nonlinear, and thus dependent on the signal. Furthermore, the CDU implementation on the transistor level can be rather complicated and thus introduce nonlinearity, offset, and frequency dependence into the CDU parameters. The circuit complexity is also responsible for higher total power consumption. On the other hand, the circuit in Fig. 2 does not suffer from such problems. It benefits from the fact that non-zero input resistances are allowed by definition but on a level that is acceptable for a given application. The fact that the impedances of p and n terminals are linear and of resistive nature up to frequency band, in which the parasitic capacitances of the OTA inputs begin to take effect, can be utilized for applications which use the fixed input resistances of the CDU for generating the transfer functions of filters [14].

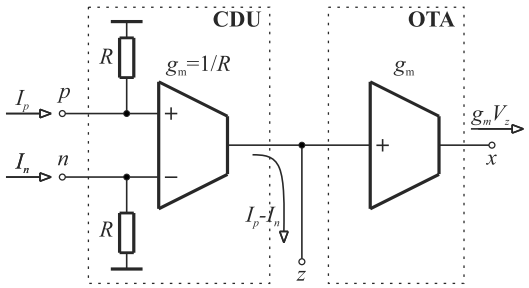


Fig. 2: Conception of the CDTA implementation.

It follows from Fig. 2 that the voltage of z terminal is transformed by another, now single-input linear OTA, into the current I_x.

With respect to the required linearity, accuracy, and high dynamic range, the OTAs may be implemented via the Howland voltage-controlled current source [15] employed by accurate rail-to-rail operational or instrumentation amplifiers. Connecting additional OTAs to the node z provides the CDTA with multiple current outputs. The direction of current I_x can be simply changed via reversing the polarity of the differential input of the Howland source. The conception in Fig. 2 therefore represents a modular approach when various versions of the CDTA, CFTA, or CITA can be obtained with the help of resistors and OTAs.

The schematic of the implemented OTA in Fig. 3 starts from the well-known Howland current pump. The instrumentation amplifier AD8226 with preset unity gain maintains its output voltage, which is a sum of the input voltage V_{in} and the voltage at the REF terminal. Since the latter voltage is a buffered voltage of the output terminal, the voltage across the resistor R_S is equal to V_{in} independently of the voltage at the output terminal, and the current I_{out} is therefore given by the ratio V_{in}/R_S.

The concrete amplifiers in Fig. 3 were selected with respect to giving preference to accuracy as is

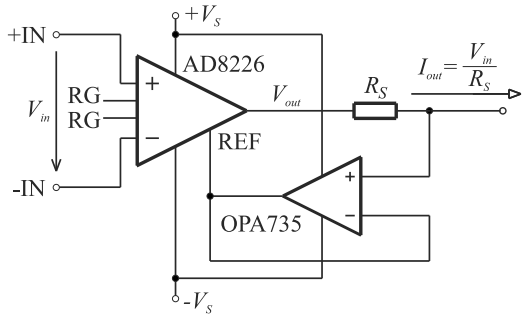


Fig. 3: OTA as the Howland current source. $V_S = \pm 5$ V. For $R_S = 100\ \Omega$, the transconductance $g_m = 10$ mS.

specified in Sec. 1. Both amplifiers have approximately the same 1.5 MHz bandwidth. For the dynamic range of processed signals, the limiting factor is the maximum power supply voltage of OPA735 (±6 V). The implemented CDTA is supplied with ±5 V. The amplifiers AD8226 and OPA735 provide low offset voltage (50 μV and 5 μV) with low drift (0.5 μV/°C and 0.05 μV/°C). The input differential impedance of the AD8226 is 800 MΩ with a parasitic capacitance of 2 pF, thus it does not degrade the output resistance of the preliminary CDU. Low input bias current (200 pA) of the OPA735-based voltage buffer represents a negligible error in setting the output current.

OPA735 provides the rail-to-rail output swing within 50 mV of the rails. More limiting for the dynamic range of the OTA is the common mode input voltage range. For 5 V power supply, the maximum common input voltage of the OPA735 is ca 3.5 V. The AD8226 is also specified as a rail-to-rail output amplifier, with the input range depending on the common and differential voltages and on the voltage at REF terminal. Both amplifiers provide the ability to go with the input voltage 0.1 V below the negative supply.

The high CMRR (more than 90 dB) and 0.01 % accuracy of internal gain resistors of AD8226 as well as the high open-loop gain of OPA735 (130 dB) are good prerequisites for a reasonably high output impedance of the Howland current source.

4. Analysis of Real Effects

As follows from Fig. 2, each sensing resistor $R = 100\ \Omega$ in the p and n inputs is loaded with high-impedance input of OTA with 2 pF parasitic capacitance, which provides a parasitic pole in the transfer function with a cutoff frequency of 800 MHz, thus absolutely beyond the CDTA bandwidth.

As regards the analysis of real effects of the current source in Fig. 3, there are some results available in papers dealing with various versions of the Howland pump [16]. Let us focus on the DC analysis of the key parameter, the internal resistance of the current source $R_i = V_{out}/I_{out}$ (see Fig. 4). It is useful to start from the simplified schematic of the difference amplifier, which is a part of the instrumentation amplifier AD8226. The nominal value of the resistors R_1 to R_4 in Fig. 4 is $R_N = 50\ k\Omega$, and their precision dramatically affects the internal resistance. Suppose that the open loop gain of OPA1 is sufficiently high and therefore it does not influence the precision of the output current. Then the output resistance can be substantially influenced by the parameters of other components within the feedback loop, namely by the resistance R_S, gain A_b of the buffer employing OPA2, and the common-voltage gain A_{cm} of OPA1. A routine analysis yields the formula for the internal resistance:

$$R_i = \frac{R_S}{1 - A_b \dfrac{1 + A_{cm} + \dfrac{R_2}{R_1}}{1 + \dfrac{R_4}{R_3}}}. \tag{2}$$

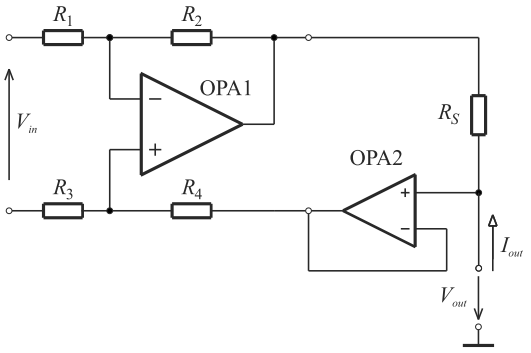


Fig. 4: Simplified OTA schematic with denoted difference amplifier with OPA1 as a part of the instrumentation amplifier AD8226 for analysing the output resistance V_{out}/I_{out}.

In the ideal case, i.e. for $A_{cm} = 0$, $A_b = 1$, and $R_1 = R_2 = R_3 = R_4 = R_N$, the internal resistance is infinite.

Consider the variances of the resistances R_1 to R_4 about the nominal value $R_N = 50$ kΩ:

$$\begin{aligned} R_k &= R_N + \Delta R_k = R_N(1 + \delta_k), \\ \delta_k &= \frac{\Delta R_k}{R_N}, \\ k &= 1 \ldots 4. \end{aligned} \tag{3}$$

Equation (2) can then be rewritten in the form:

$$R_i = \frac{R_S}{1 - A_b \dfrac{1 + A_{cm} + \dfrac{1 + \delta_2}{1 + \delta_1}}{1 + \dfrac{1 + \delta_4}{1 + \delta_3}}}. \tag{4}$$

Let us perform the worst-case analysis for the amplifier AD8226, whose internal resistances R_1 to R_4 are made with an error below 0.01 %, thus:

$$|\delta_k| = \delta_{\max} = 10^{-4}, \quad k = 1 \ldots 4. \tag{5}$$

The worst case, the lowest possible resistance $R_{i,\min}$, occurs for $\delta_1 = -\delta_2 = -\delta_3 = \delta_4 = \delta_{\max}$. Substituting this condition into Eq. (2) and arranging yield:

$$R_{i,\min} = \frac{R_S}{1 - A_b(1-\delta_{\max})\left[\dfrac{A_{cm}}{2} + \dfrac{1}{1+\delta_{\max}}\right]}. \tag{6}$$

If the variation of the fixed sensing resistor R_S is not considered, then the internal resistance depends on the gains A_{cm} and A_b. Since the common mode rejection of the AD8226 is higher than 90 dB, $A_{cm} < 3.16 \cdot 10^{-5}$. The buffer employs the OPA735 with an open-loop gain of 130 dB, thus $A_0 = 3.16 \cdot 10^6$, and therefore $A_b = A_0(1 + A_0) = 0.999999684$. These numbers, projected into Eq. (6), demonstrate the negligible impact of A_{cm} and A_b of AD8226 and OPA735 on the result. Then:

$$R_{i,\min} \approx \frac{R_S}{1 - \dfrac{1-\delta_{\max}}{1+\delta_{\max}}} = \\ = \frac{R_S}{2}\left(1 + \frac{1}{\delta_{\max}}\right) \approx \frac{R_S}{2\delta_{\max}}. \tag{7}$$

For a maximum resistance error of 0.01 %, the estimated lowest internal resistance is 5000 R_S, thus 500 kΩ. The measurements on implemented CDTA confirm values above 800 kΩ (see Sec. 5.).

Note the high sensitivity of the internal resistance to the buffer gain A_b in Eq. (6). This goes to show the importance of the high open loop gain of the OpAmp which implements the buffer. For example, a low gain of 10000 would result in lowering the A_b to 0.9999 and decreasing the internal resistance of the source to 3300 R_S. That is why one must reckon with decreasing internal resistance for higher frequencies where the OpAmp gain goes down.

On the other hand, Eq. (4) can be used for deriving the condition of DC (in)stability of the circuit. For a stable circuit, the internal resistance must be positive. The stability condition reads:

$$A_b < \frac{1 + \dfrac{1+\delta_4}{1+\delta_3}}{1 + A_{cm} + \dfrac{1+\delta_2}{1+\delta_1}}. \tag{8}$$

For the Howland circuit to be DC stable for all possible variations of the errors (Eq. (3)), the condition (Eq. (8)) would have to be fulfilled also for $-\delta_1 = \delta_2 = \delta_3 = -\delta_4 = \delta_{\max}$, or:

$$A_b < \frac{1-\delta_{\max}}{1+\delta_{\max}} \frac{1}{1 + A_{cm}\dfrac{1-\delta_{\max}}{2}} \approx \frac{1-\delta_{\max}}{1+\delta_{\max}}. \tag{9}$$

The latter simplified formula holds for $A_{cm} \ll 1$.

For $\delta_{\max} = 10^{-4}$, $A_b < 0.9998$, which would represent the buffer implementation by an OpAmp with a nonrealistic low open-loop gain of 5000. The internal resistance (Eq. (4)) would then be very low. On the contrary, utilizing an accurate high-gain OpAmp can, for unfavorable spread of the resistance values of AD8226, lead to instability. It can be derived from Eq. (9) that, utilizing the OPA735, the Howland circuit would surely be stable for any arbitrary resistive errors with unrealistically low $\delta_{\max} = 1.58 \cdot 10^{-7}$. The circuit optimization with the aim of maximizing R_i and concurrently preserving stable behavior is possible via experimental trimming of resistances, but with the instrumental amplifier built from classical OpAmps and accurate resistors [15].

The symbolic analysis of the circuit in Fig. 4, made with the linear one-pole models of both OpAmps, provides the following results (the proofs are given in the Appendix):

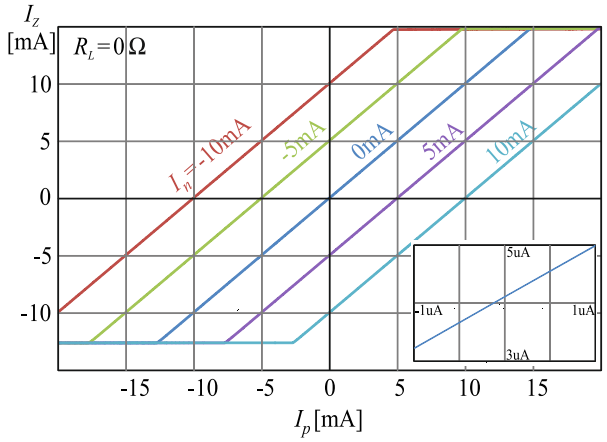
- The output impedance exhibits two real poles, which do not depend on R_S and on the impedance level R_N of resistors R_1 to R_4.
- The output impedance is equal to R_i according to Eq. (4) for zero frequency, and it converges to R_S for frequencies tending to infinity.
- The output impedance contains a capacitive part, which should be considered when designing applications which employ the implemented CDTA.
- The positive (negative) R_i is the necessary and also sufficient condition of the stability (instability) of the Howland circuit.

5. Measurements on Implemented CDTA

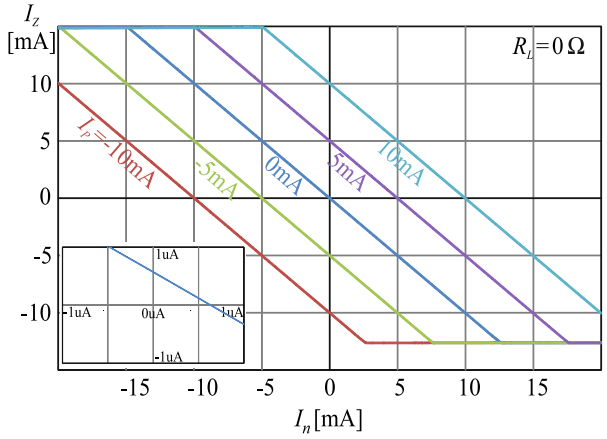
This section summarizes the results of DC and AC measurements on the CDTA, implemented according to Fig. 3 and Fig. 4 with the parameters $R_p = R_n = R_S = 100\ \Omega$ and $V_S = \pm 5\ V$. The DC characteristics were measured using the parametric analyzer B1500A and the frequency responses by the network analyzer E5061B, both made by Keysight Technologies, Inc.

Figure 5, Fig. 6, and Fig. 7 show the CDU measurements.

Figure 5 provides the DC characteristics I_z vs I_p with the current I_n as a parameter, and I_z vs I_n with the current I_p as a parameter. Both types of characteristics were measured with the z terminal grounded (zero R_L load resistance). For the p terminal, the current offset and positive and negative saturation levels were 4 µA, −14.5 mA, and 12.5 mA. For the n terminal, these values were 0.6 µA, −12.5 mA, and 14.5 mA. Note the excellent linearity of all the characteristics.



(a) $I_z(I_p)$, parameter I_n.

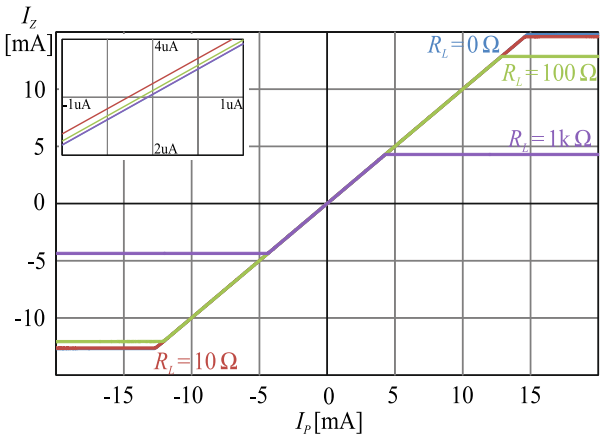


(b) $I_z(I_n)$, parameter I_p.

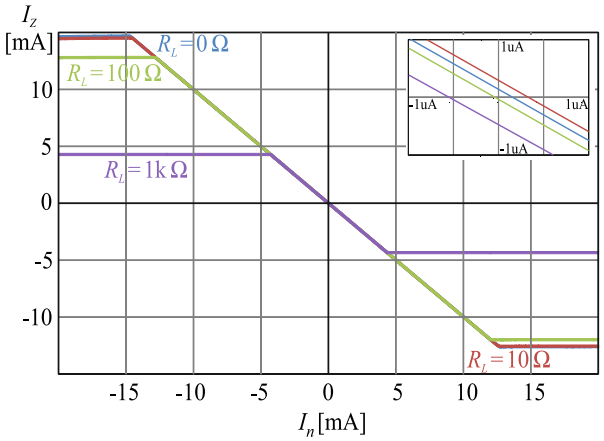
Fig. 5: CDU: DC characteristics.

The characteristics I_z vs I_p and I_n in Fig. 6 were measured for various loads connected to the z terminal. The saturation levels now depend on the voltage V_z, which appears on the load due to the flowing current I_z. When driving the p terminal, the maximum offset (3.16 µA) was measured for a load of 10 Ω. For the n terminal, the maximum offset (0.4 µA) was for $R_L = 1$ kΩ.

Figure 7 summarizes AC measurements on the CDU, namely the Amplitude (A) and Phase (P) frequency responses of current gains from the p or n terminal to the grounded z terminal. The cutoff frequency from



(a) $I_z(I_p)$, $I_n = 0$, parameter R_L.



(b) $I_z(I_n)$, $I_n = 0$, parameter R_L.

Fig. 6: CDU: DC characteristics.

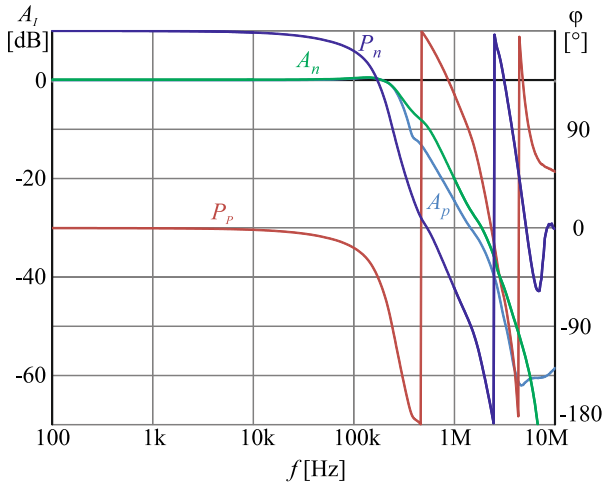


Fig. 7: AC characteristics of CDU: Amplitude (A) and Phase (P) frequency characteristics from p and n to z terminal.

the p and the n terminal is 275 kHz and 285 kHz, respectively.

The DC transconductance characteristic, i.e. the output current I_{out} vs the input voltage V_{in}, can be easily obtained from Fig. 6(a) after a simple transformation of axes: $I_{out} = I_z$ and $V_{in} = R \cdot I_p$, where $R = 100\ \Omega$. Then, for $R_L = 0$, the OTA saturates for $V_{in} \approx 1.5$ V.

The DC internal resistance of the OTA current output is 883 kΩ. It was read from the characteristic I_{out} vs V_{out} measured according to Fig. 4.

The frequency response of the OTA, i.e. the transconductance vs frequency, can be obtained from the curves in Fig. 7, where the level of 0 dB corresponds to the value $g_m = 1/R = 100$ mS. The bandwidth is 525 kHz.

6. Benchmark Circuit - CDTA Biquad

The implemented CDTA was used in the 2nd order filter in Fig. 8, and the filter operation was tested via AC, DC, and transient measurements. This circuit was designed on the basis of similar filter with the Current-Controlled Current Differencing Buffered Amplifier (CC-CDBA), published in [14], where the parasitic resistances of p and n terminals of the CDU were used for implementing the required transfer functions. The circuit in Fig. 8 profits from two effects:

- the resistors R_1 and R_2 are parts of the implemented CDTA,
- the output buffer is also a part of the CDTA (OPA 735 in the Howland source in Fig. 3).

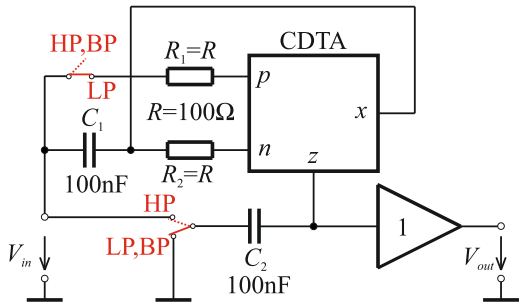


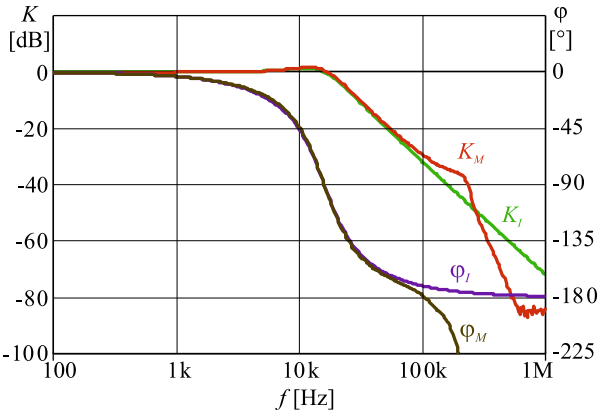
Fig. 8: Biquad based on a single CDTA.

The transfer functions of the filter are as follows:

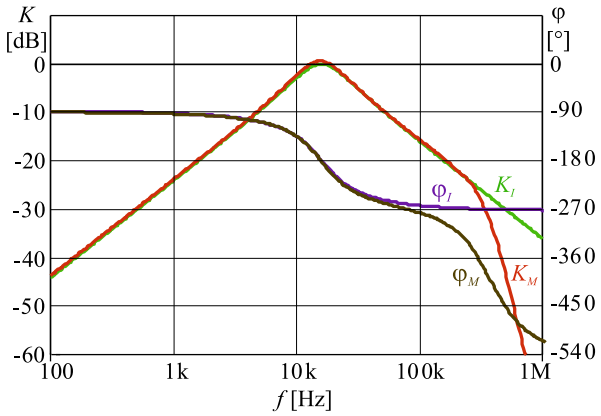
$$\begin{aligned} \frac{V_{LP}}{V_{in}} &= \frac{N_{LP}(s)}{D(s)}, \\ \frac{V_{BP}}{V_{in}} &= \frac{N_{BP}(s)}{D(s)}, \\ \frac{V_{HP}}{V_{in}} &= \frac{N_{HP}(s)}{D(s)}, \end{aligned} \tag{10}$$

where

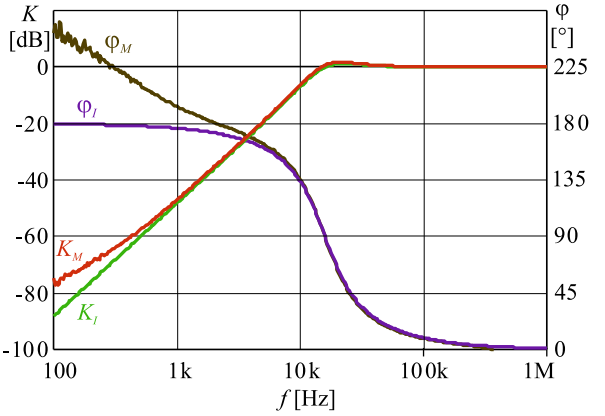
$$\begin{aligned} D(s) &= s^2 R_2 C_1 C_2 + s C_2 + g_m, \\ N_{LP}(s) &= \frac{1 + sC_1(R_2 - R_1)}{R_1}, \\ N_{BP}(s) &= -sC_1, \\ N_{HP}(s) &= s^2 R_2 C_1 C_2 + s(C_2 - C_1). \end{aligned} \tag{11}$$



(a) LP.



(b) BP.



(c) HP.

Fig. 9: Ideal (K_I, φ_I) and measured (K_M, φ_M) frequency responses of LP, BP, HP filter from Fig. 8.

The natural frequency and quality factor are:

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{g_m}{R_1 C_1 C_2}}, \qquad Q = \sqrt{g_m R_1 \frac{C_1}{C_2}}. \tag{12}$$

For the parameters proposed in the implementation, namely $C_1 = C_2 = 100$ nF, $R_1 = 100\ \Omega$, $g_m = 10$ mS, f_0 and Q are 15.9 kHz and 1, respectively. Note that to achieve low-pass or high-pass response, the condition $R_1 = R_2$ or $C_1 = C_2$ must be fulfilled.

The measured frequency responses in Fig. 9 are in a good accordance with the design objectives. It follows from a comparison of ideal and measured responses that the implemented CDTA can satisfactorily operate in this application within a frequency range of up to hundreds of kHz. The parasitic low-frequency phase shift of the high-pass section is caused by mismatched capacitances $C_1 = 110$ nF and $C_2 = 106$ nF, whose difference generates additional transfer zero according to Eq. (11).

7. Conclusion

Based on the concept of the Howland current pump, the CDTA implementation via commercial ICs is proposed. Attention is paid to the accuracy and maximum dynamic range of processed signals. The measurements confirmed a high linearity of DC characteristics of the CDU and OTA. On the other hand, the weak point of the Howland source is the high sensitivity of its internal resistance to variations of resistances in the difference amplifier and the possibility of unstable behavior, as well as a sharp decrease in internal impedance with increasing frequency. These real influences are analyzed in detail. It is shown that the bandwidth of this impedance is the smaller, the higher the DC internal resistance that can be adjusted via trimming the resistors in the difference amplifier. A frequency model of the internal impedance is found. It turns out that the bandwidth of the Holland source is governed by its DC internal resistance and by a capacitance which is indirectly proportional to the bandwidth of the OpAmps in the source. It is therefore advisable to focus on overcoming these fundamental limitations in constructing the wideband controlled current sources, and searching for more acceptable circuit solutions providing higher bandwidths than the Howland source can offer, though at the cost of lower internal impedances.

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Appendix A

Consider the following transfer functions K_1 and K_2 of the OPA1 and OPA2 amplifiers in the model from Fig. 4:

$$K_1 = \frac{\omega_1}{s}, \qquad K_2 = \frac{A_b}{1 + \frac{s}{\omega_2}}. \tag{13}$$

Here, K_1 is a model of high-gain OpAmp (a part of the instrumentation amplifier) with the bandwidth ω_1 corresponding to the bandwidth of unity-gain instrumentation amplifier, and K_2 models the voltage buffer in Fig. 4, where $A_b \approx 1$ and ω_2 is the cutoff frequency, which corresponds to the GBW of the utilized OpAmp.

The symbolic analysis of the internal impedance Z_i of the current source leads to the formula:

$$Z_i = R_S \frac{a_2 s^2 + a_1 s + a_0}{a_2 s^2 + a_1 s + a_0 - b_0}, \tag{14}$$

where

$$\begin{aligned} a_0 &= \omega_1\omega_2 R_1 (R_3 + R_4), \\ b_0 &= \omega_1\omega_2 A_b R_3 (R_1 + R_2), \\ a_1 &= \omega_2 S_p + A_b\omega_1 R_1 (R_3 + R_4), \\ a_2 &= A_b S_p, \\ S_p &= R_1R_3 + R_1R_4 + R_2R_3 + R_2R_4. \end{aligned} \tag{15}$$

For $s = 0$, Eq. (14) yields Eq. (2) for DC resistance R_i while neglecting the common-mode gain A_{cm}:

$$R_i = R_S \frac{a_0}{a_0 - b_0} = \frac{R_S}{1 - A_b \dfrac{1 + \dfrac{R_2}{R_1}}{1 + \dfrac{R_4}{R_3}}}. \tag{16}$$

The determinant of the quadratic equation in the denominator of Eq. (14) is always positive:

$$\begin{aligned} &a_1^2 - 4a_2 (a_0 - b_0) = \\ &= (\omega_2 S_p - A_b\omega_1 R_1 (R_3 + R_4))^2 + \\ &+4A_b^2 S_p \omega_1\omega_2 R_3 (R_1 + R_2) > 0. \end{aligned} \tag{17}$$

The circuit therefore exhibits two different real poles, and the current response to the steps in the load or the OTA input will be monotonic without overshoots. The sufficient condition of the stability, i.e. for both poles to be negative, are positive coefficients a_2, a_1, and a_0 - b_0 in the denominator of Eq. (14), or $a_0 > b_0$. As is obvious from Eq. (16), it is equivalent to the condition $R_i > 0$. The positive DC internal resistance therefore guarantees the stability.

It follows from Eq. (14) that for high frequencies, thus for $s \to \infty$, the impedance falls to R_S. The way this happens is given by the Z_i model in Fig. 10, which can be derived by the following arrangement of Eq. (14):

$$Z_i = R_S + \frac{1}{\dfrac{1}{R_{eq}} + sC_{eq} + s^2 D_{eq}}, \tag{18}$$

where

$$\begin{aligned} R_{eq} &= R_i - R_S, \\ C_{eq} &= \frac{a_1}{b_0 R_S}, \\ D_{eq} &= \frac{a_2}{b_0 R_S}, \end{aligned} \tag{19}$$

are parameters of the resistor, capacitor, and Frequency Dependent Negative Resistor (FDNR) in Fig. 10. For low frequencies, the impedance is $R_S + R_i - R_S = R_i$. If the frequency increases, the resistor $R_i - R_S$ is gradually shunted by the capacitor C_{eq} whose susceptance increases proportionally with the frequency. As a second-order effect, the negative conductance of shunting FDNR, increasing with the square of frequency, decreases the total resistivity of the parallel configuration. However, it does not affect the final drop of the impedance of this parallel subcircuit towards zero, when Z_i tends to R_S. As the simulation confirms, C_{eq} is the dominant element for the frequency dependence of Z_i, and the FDNR only modifies this dependence in the frequency area where the impedance is already suppressed. For practical computation, for example for estimating the bandwidth of the Z_i, the schematic in Fig. 10 can be simplified via removing the FDNR.

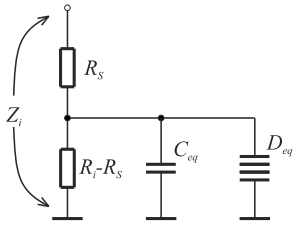

Fig. 10: Impedance model of the Howland circuit.

Considering that R_1 to R_4 are accurate resistors, thus $R_1 \approx R_2 \approx R_3 \approx R_4 \approx R$, and that $A_b \approx 1$, then the capacitance C_{eq} from Eq. (19) can be estimated as:

$$C_{eq} \approx \frac{1}{R_S}\left(\frac{2}{\omega_1} + \frac{1}{\omega_2}\right). \tag{20}$$

For the Howland pump with AD8226 and OPA735 and with $R_S = 100\ \Omega$, the equivalent capacitance is about 3 nF. It may not be a problem if this source is used in the OTA stage of the CDTA since the current terminal x is usually connected to a low-impedance node. A worse case can occur with the OTA as a part of the CDU: a grounded capacitor is frequently connected to the corresponding z terminal. Then its capacitance should not be less than ca $10 \cdot C_{eq}$.

It follows from Fig. 10 that the cutoff frequency of the impedance is governed by the cutoff frequency ω_c of the corresponding RC cell, thus:

$$\omega_c \approx \frac{1}{R_i C_{eq}} \approx \frac{R_S}{R_i} \frac{1}{\dfrac{2}{\omega_1} + \dfrac{1}{\omega_2}}. \tag{21}$$

It reveals the disadvantage of the Howland circuit: the higher the internal resistance R_i will be adjusted via optimizing the resistive network R_1 to R_4, the lower the bandwidth will be, and the closer to the instability region the circuit will be.