A Simple SVM Technique on Three-Phase MPUC7 Inverter for Solar Photovoltaic System

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Abstract. *In This paper, a simple single-dimension Space Vector Modulation (SVM) technique is introduced to implement on three-phase thirteen-level Modified Packed U-Cell (MPUC) inverter for photovoltaic system in which many DC sources are available. The three-phase thirteen-level converter consists of three single-phase seven-level MPUCs that each phase has six switches and two isolated DC sources. One major advantage of proposed method is to produce an output voltage with nearly constant amplitude in desired range in case of input DC voltage fluctuations, which is common in renewable sources like Photovoltaic Systems (PV). On the other hand, the conventional Pulse Width Modulation (PWM) strategies do not have such capability. Thus, the converter behavior is investigated for the proposed control method and Level Shift PWM (LS-PWM) and it is shown that the LS-PWM method does not function properly when the DC voltage varies. In order to produce an output voltage with seven equal levels, which results in reduction of the switching losses and Total Harmonic Distortion (THD), it is necessary to trigger switches in proper way. Consequently, two switching patterns are introduced and the significant decrease in power loss due to the second switching pattern is shown. Furthermore, it is investigated that in three-phase mode, the 3rd order line-voltage harmonics are eliminated well and the voltage and current THD are further improved by the proposed method. To validate the proposed SVM technique, MATLAB Simulink simulation results are presented and a comparative analysis is done between the proposed method and LS-PWM.*

Keywords

Level Shift Pulse Width Modulation (LS-PWM), modified packed U-cell, MPUC7, multilevel inverter, space vector modulation, solar photovoltaic system.

1. Introduction

Recent developments in renewable energy resources oblige the power grid authorities to develop and implement the high efficiency low cost technologies as interface between the grid and new energy sources like Photovoltaic Systems (PV), wind turbines, fuel cells and etc. [1] and [2]. Power converters are used for power conversion between renewable energies and grids or standalone loads. The power electronic converters affect the power quality of the system. Consequently, the power quality is a controversial issue in design and manufacturing of the converters. Furthermore, the number of semiconductor switches and capacitors has made a competitive market for manufacturers. On the other hand, generating more voltage levels at the output of the converter results in lower harmonic contents and smaller size of output filters, which reduces the cost and the size of the converter. So, the use of multilevel inverters is inevitable to meet the needs of high power quality demands and competitive renewable power resource markets [3] and [4].

Various topologies have been introduced in the field of multilevel converters. Single-DC source 7-level Cascaded H-Bridge (CHB) inverter is introduced in the [5],

which has advantages such as modular structure and appropriate power quality, but its main drawback is the use of large number of switches and the need for a complex controller to stabilize the capacitor voltage. Packed U-cell inverter or PUC is an emerging candidate to replace the traditional inverters like CHB, Flying-Capacitor (FC) or Neutral Point Clamped (NPC) having lower component counts especially DC sources and capacitors. It was introduced by Al-Haddad as a seven-level single phase inverter having just six active switches, one DC source and a capacitor as the auxiliary DC link [6]. But the complex voltage balancing of the DC link capacitor as well as using high number of sensors were its main drawbacks. So, the five-level topology is introduced without any sensors and closed loop controllers for DC link capacitor balancing, just by using the proper switching technique [7].

Afterwards, different topologies of PUC for generating different voltage levels using a variety of switching technologies were introduced in literatures. Besides, one major disadvantage of PUC was the amplitude of the output voltage, which was limited to the DC source level. In fact, PUC could not generate an output voltage with a higher amplitude than the DC source. So, the modified topology or Modified Packed U-Cell (MPUC) was introduced with the ability of voltage boosting by replacing the DC link capacitor with DC independent source, which many of them are available in solar power systems with different voltages. MPUC inverter is very applicable in field of renewable energy conversion. In this topology, two different solar arrays are connected to MPUC inverter as DC input sources through boost converters.[8] Furthermore, lower switching frequency and voltage rating of switches are the other advantages of the MPUC inverter that are discussed in the literature [9] and [10].

To reach lower voltage and current Total Harmonic Distortion (THD) contents, the modulation technique takes the most important rule. Amongst the multicarrier Pulse Width Modulation (PWM) schemes, two of them are more useful in PUC inverter: Level Shift Pulse Width Modulation (LS-PWM) and Phase Shifted Pulse Width Modulation (PS-PWM) [3]. Several types of modulation techniques are investigated by some authors for implementing on PUC inverter. However, the main disadvantage of all those methods is the lack of proper control on the output voltage in case of changes in the DC input source voltage, which leads to increase in the THD and decreases the accuracy of control for creating a reference waveform in the converter output.

Space Vector Modulation (SVM) technique can simply be implemented on digital microcontrollers, so this technique is becoming more popular over sinusoidal PWM and recently has received more attention for multilevel converters application [11] and [12]. The space vector modulation could be a solution to stabilize the output voltage in case of having any variation at the input DC source but it is not applicable by sinusoidal PWM techniques, in which the reference voltage has no effect on calculation of the trigger times of switches. Also, different objectives such as power losses, THD minimization or elimination, can be integrated into the dwell time calculations to choose proper switching states. SVM technique was introduced for three phase inverters by vectors moving at two dimensions, while some simple methods thereafter introduced for single phase systems called as 1-D-SVM [13] and [14].

This study is dedicated to investigate the operation of a seven-level modified PUC inverter hereafter called MPUC7, for solar PV systems using simplified SVM and level-shift PWM techniques to present a comparative analysis from the point of view of THD contents, power losses and stabilization of output voltage in case of having DC voltage source fluctuations. The structure and switching states of single phase MPUC7 is reviewed in Sec. 2. Also, the structure of three-phase topology is introduced in the same section. Then in Sec. 3. , the proposed SVM method design procedure is explained for three-phase MPUC7 and the algebraic equations are explained to find the dwell times of vectors. And, two switching sequences for this method are introduced and compared from the point of view of generating lower THD contents and power losses. Then the simulation results are discussed in Sec. 4. The waveforms of current and voltage and the harmonic spectrum are investigated. And the ability of inverter to produce stabilized output voltage in case of DC source variations are presented. Furthermore, the switching losses are compared for the proposed method and LS-PWM techniques to show lower losses in this method. In the end, conclusions are presented in Sec. 5.

2. Seven-Level Modified Packed U-Cell Inverter

As mentioned earlier in Sec. 1. , the new emerging PUC7 inverter is the most promising topology among the other conventional multilevel inverters like NPC, FC or even CHBs, which are more popular amongst the power industries because of their modular design. PUC has the advantages of both FC and CHB inverters. Despite the interesting characteristics, the need for complex control techniques for DC link capacitor balancing in addition to lack of boosted output voltage made it difficult to reach wide spread acceptance from the market and industries. Actually, the maximum value of amplitude of voltage available at the out-

put of PUC is limited to the maximum amplitude of DC source voltage level. So, it does not seem to be appropriate for medium or high power applications [15] and [16].

Nowadays, by advancements in PV systems and more economic costs of solar panels, a variety of isolated DC sources are available [17]. So, using large number of DC sources does not seem as a negative point for multilevel inverters. Having more DC sources available, the modified PUC or MPUC was introduced using multiple DC sources without any capacitors, producing a voltage by amplitude more than the maximum of DC input sources of PUC, which was its main drawback [18]. The MPUC7 topology is shown in Fig. 1. The next difference with respect to PUC is the reversed direction of DC source V_2. Also, the lower switches S_3 & S_6 are reversed to hinder current through diodes. So, by using appropriate gate pulses, the current flow path can be hindered or allowed. Table 1 shows various switching states as well as output voltage levels of MPUC7. As it can be seen, the maximum output voltage level generated by MPUC is the sum of two DC sources i.e. $V_1 + V_2$, which is obtained by connecting two voltage sources in series. By connecting two DC sources in series, the voltage level $V_1 + V_2$ is obtained. By making second voltage source appear on the load, the voltage level V_2 is achieved. V_1 voltage level can be achieved by connecting first voltage source to the load. Thus, producing more voltage level amplitudes is feasible by this topology. That is obvious from the Tab. 1. that by choosing the first DC source (V_1) amplitude, which is two times the second DC source (V_2) amplitude i.e. $V_1 = 2 \cdot V_2$ ($V_2 = E$), seven uniform voltage levels are generated at the output of inverter. So, the output voltage levels are: 0, E, $2E$, $3E$. Therefore, the maximum output voltage level is equal to $3E$ while the maximum DC source is $2E$.

Tab. 1: Switching states & voltage Levels of MPUC7 inverter.

Switching state	S_1	S_2	S_3	S_4	S_5	S_6	V_L
1	1	0	1	0	1	0	$V_1 + V_2$
2	1	0	0	0	1	1	V_1
3	0	0	1	1	1	0	V_2
4	0	0	0	1	1	1	0
5	1	1	1	0	0	0	0
6	1	1	0	0	0	1	$-V_2$
7	0	1	1	1	0	0	$-V_1$
8	0	1	0	1	0	1	$-V_1 - V_2$

There are two redundant voltage states (states 4 & 5), which generate the zero-voltage level at the output and are used to reduce the switching frequency. When it is required to produce zero voltage level, by choosing the appropriate state between states 4 and 5 with the modulation technique, less change happens when turning on & off mode in switches, which reduces the switching frequency. From Tab. 1, one can conclude that two switches S_2 and S_5 operate at the line frequency irrespective of switching and carrier frequencies.

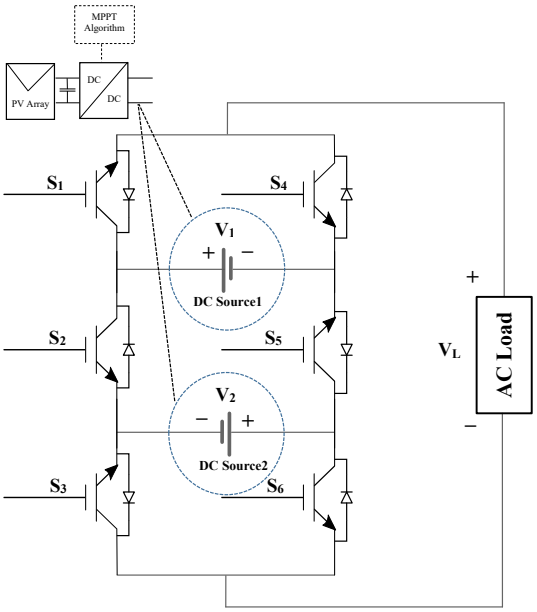


Fig. 1: MPUC inverter topology.

Table 2 shows a comparison between the components count for single-phase 7-level inverters. As can be seen, the PUC and MPUC topologies have the least number of components while generating the same voltage levels. In addition, the PUC family does not have the complexities of FC and NPC for capacitor or neutral point balancing especially in high levels of output waveform. Furthermore, by the new economic solar panel ratings available in the market, having a greater number of DC sources would not be a matter of concern and so, the use of MPUC would be more satisfactorily because of no capacitor balancing problems in comparison to traditional PUC [19].

2.1. Three-Phase MPUC7

The configuration of three-phase MPUC7 is shown in Fig. 2. It consists of 3 single-phase MPUC7 units including total number of 6 isolated DC sources and 18 switches. The neutral point could be floating or connected to the loads. So, the 3-phase MPUC7 topology can be used for both 3-wire and 4-wire systems. It can deliver renewable energy to a 3-phase electric grid or run a three -phase motor as 3-wire applications. Also, the neutral point can be used as fourth wire. So, it would be appropriate for UPS applications to feed single-phase or three-phase loads simultaneously as a 4-wire system.

Tab. 2: Components count.

Switching	DC source	Capacitor	Clamped diode	Active switch	Total
CHB with equal DC sources	3	0	0	12	15
Diode-Clamped inverter	1	6	30	12	49
FC	1	21	0	10	32
PUC7	1	1	0	6	8
MPUC7	2	0	0	6	8

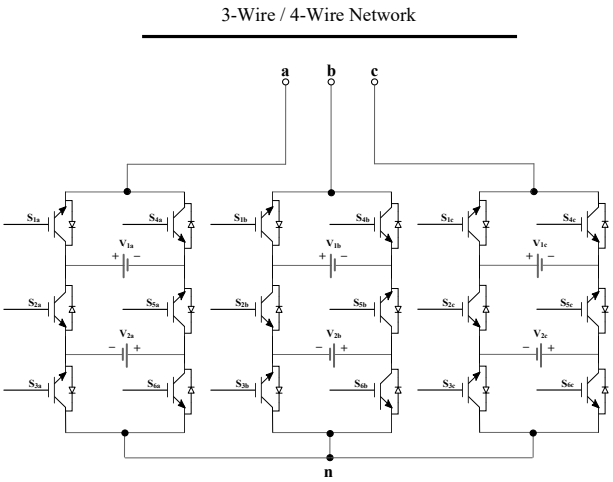


Fig. 2: Three-phase MPUC7 topology.

3. Simplified SVM for Three-Phase MPUC7

SVM uses voltage vectors to produce the reference voltage. Reference voltage is a desired output voltage, which should be produced by the inverter, while voltage vectors are real output voltages that are generated with the different states of switches. By selecting proper switching states from the valid ones of the converter and by calculating the proper time periods that they should be used in, the reference voltage in each sampling period would be generated [4]. In the proposed SVM technique, the vectors move at only one dimension instead of two dimensions [20]. For a single-phase converter, the control regions can be represented by the voltage vectors for every possible switching state, which the reference voltage vector moves through them. This method can be separately used for all three-phases, instead of the complicated conventional SVM for three-phase structure. In this method, to sectionalize the control region, the voltage levels of MPUC7 and their equivalent state vectors are used, so the number of regions is identified by following equation:

$$N_R = m - 1, \tag{1}$$

where N_R and m are the number of the regions and the voltage levels of converter, respectively. Each region is located between two state vectors and the reference vector moves through these regions. In each region, two adjacent state vectors are used to produce the reference voltage vector. As the two-level inverter, the SVM algorithm for the MPUC7 is also based on "volt-second balancing" principle [4], in which, the product of sampling period T_s and the reference voltage V_{ref} is equal to sum of the voltages multiplied by the time interval of chosen space vectors. So, the reference voltage V_{ref} is synthesized by two stationary vectors. The dwell time for the stationary vectors represents the duty-cycle time (on-state or off-state time) of the chosen switches during one sampling period of the modulation scheme. Assuming the sampling period T_s to be small enough, the reference vector V_{ref} can be considered constant during T_s.

The relations between reference vector, state vectors and corresponding dwell times for each sampling period time can be formulated as follow:

$$V_{ref} \cdot T_s = V_1 \cdot T_1 + V_2 \cdot T_2, \tag{2}$$

$$T_s = T_1 + T_2, \tag{3}$$

where V_{ref} is the reference voltage vector, V_1 and V_2 are the state vectors generating voltage levels of each region. T_s is the period of the sampling time, T_1 and T_2 are the dwell times corresponding to V_1 and V_2, respectively. So, in each region this equation should be calculated for each T_s.

Another parameter for SVM technique is the modulation index, which is given as:

$$m_a = \frac{V_{ref}}{V_{DC}}, \tag{4}$$

where V_{ref} is the voltage that should be generated at the output of inverter and V_{DC} is the sum of input DC voltage sources. As in MPUC7, the maximum level output voltage has been increased in comparison to PUC7, so a reference voltage with larger amplitude than the maximum DC input sources can be produced at the output of converter.

The control method for three-phase MPUC7 is actually an extension of the one introduced for single-phase MPUC7. So, in order to produce 3-phase 120° out-of-phase load voltages, three modulating signals that are 120° out of phase are used. The three reference signals are sinusoidal signals with equal amplitude but a relative phase shift of 120°.

3.1. Analysis of MPUC7 State Vector Regions and Dwell Times

According to Eq. (1), Six regions are drawn in Fig. 3 to show the state vectors and switching states of seven voltage levels of MPUC7 inverter. From this figure, it is referred that there are eight possible switching states for MPUC7 inverter to produce a seven-level output voltage. For example, the switching state (1,0,1) corresponds to the case that semiconductor switches S_1, S_5, and S_3 are conducting.

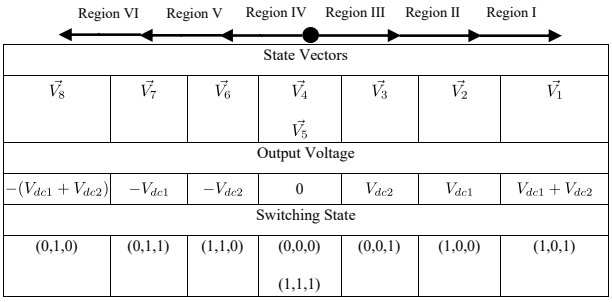


Fig. 3: State vector diagram.

As mentioned before, the reference vector V_{ref} can be synthesized by two nearest stationary vectors in each region. So, when the reference voltage locates in each region, it is generated by the combination of two adjacent voltage vectors in that region multiplied by corresponding duty cycles. Also, in order to achieve lower power losses and reduce the THD, it is important to select the sequence of switching states appropriately. In the next section, this issue is described by details. For example, by using the "Three-Segment Switching" sequence, when the reference voltage vector falls into region I as shown in Fig. 3, it is synthesized by vectors V_1 and V_2. So the volt-second balancing equation is as follow:

$$V_{ref} \cdot T_s = V_1 \cdot T_a + V_2 \cdot T_b, \tag{5}$$

$$T_s = T_a + T_b. \tag{6}$$

In this region, vector V_1 generates voltage 3E and vector V_2 produces voltage 2E at the output of MPUC7. Actually, if the reference voltage is located between 2E and 3E, the corresponding vectors of this region by the following duty cycles should be activated:

$$V_{ref} \cdot T_s = 3E \cdot T_a + 2E \cdot T_b, \tag{7}$$

$$T_a = T_s \cdot \left(\frac{V_{ref}}{E} - 2 \right), \tag{8}$$

$$T_b = T_s \cdot \left(3 - \frac{V_{ref}}{E} \right), \tag{9}$$

where T_a and T_b are the corresponding duty cycles of V_1 and V_2, respectively. From Eq. (7), Eq. (8) and Eq. (9), it is obvious that the values of the duty cycles T_a and T_b are related to the values of the amplitude of V_{ref} and input DC voltage sources. As the value of the DC voltage sources may change in case of using solar panels, so by the proposed SVM method, the effect of these changes is minimized on the converter output. Due to this feature, this method extends the input voltage range of the PV system and allows simple implementation of Maximum Power Point Tracing (MPPT) algorithm for a wide range of operating points. As the changes of solar radiation and temperature influence the characteristics of the PV modules, so MPPT is an important issue for PV systems. Amongst the MPPT methods, the P&O algorithm is comprehensively applied by the industries [21]. Moreover, the relevant costs of the DC link voltage controller or the complicated MPPT systems could be reduced [22] and [23]. Another important point is the normalized sampling frequency. The normalized sampling frequency is defined by Eq. (10):

$$m_f = \frac{F_s}{F_n}, \tag{10}$$

where F_s is the sampling frequency and F_n is the frequency of the reference voltage signal. It has been proven in order to reduce harmonic contents in the output waveforms, the normalized sampling frequency should be selected as the integer multiple of the number 6 [24]. So the number of sampling periods is symmetrically distributed in six regions for each period of the reference voltage frequency. Accordingly, the voltage waveform will be symmetrical and all the regions are used symmetrically in each period and the harmonic contents in the output waveforms will decrease. Furthermore, in symmetrical three-phase system, due to the symmetry of the output pulse waveforms, the 3rd. order harmonics are well removed at the line voltage.

3.2. Switching Sequence

As mentioned before, proper selection of the sequence of switching states plays an important role to reduce the switching losses and THD. For this purpose, the switching sequence should satisfy following terms [4]:

- In transition from each switching state to another, just two switches have to be changed.
- When reference vector transfers from one region to the next, no or minimum number of switching should happen.

In this paper, to reach the best switching sequence according to the above-mentioned requirements, two switching sequences featuring the best results in terms

Tab. 3: Three-segment switching sequence.

Region	Dwell time	Switching segment		
		1 $\frac{T_a}{2}$	2 T_b	3 $\frac{T_a}{2}$
I	$T_a = T_s \cdot \left(\frac{V_{ref}-V_{dc1}}{V_{dc2}}\right)$	$\vec{V_1}$	$\vec{V_2}$	$\vec{V_1}$
	$T_b = T_s \cdot \left(\frac{V_{dc1}+V_{dc2}-V_{ref}}{V_{dc2}}\right)$	(1,0,1)	(1,0,0)	(1,0,1)
II	$T_a = T_s \cdot \left(\frac{V_{ref}-V_{dc1}}{V_{dc2}-V_{dc1}}\right)$	$\vec{V_3}$	$\vec{V_2}$	$\vec{V_3}$
	$T_b = T_s \cdot \left(\frac{V_{ref}-V_{dc2}}{V_{dc1}-V_{dc2}}\right)$	(0,0,1)	(1,0,0)	(0,0,1)
III	$T_a = T_s \cdot \left(\frac{V_{ref}}{V_{dc2}}\right)$	$\vec{V_3}$	$\vec{V_4}$	$\vec{V_3}$
	$T_b = T_s \cdot \left(\frac{V_{dc2}-V_{ref}}{V_{dc2}}\right)$	(0,0,1)	(0,0,0)	(0,0,1)
IV	$T_a = -T_s \cdot \left(\frac{V_{ref}}{V_{dc2}}\right)$	$\vec{V_6}$	$\vec{V_5}$	$\vec{V_6}$
	$T_b = T_s \cdot \left(\frac{V_{dc2}+V_{ref}}{V_{dc2}}\right)$	(1,1,0)	(1,1,1)	(1,1,0)
V	$T_a = T_s \cdot \left(\frac{V_{ref}+V_{dc1}}{V_{dc1}-V_{dc2}}\right)$	$\vec{V_6}$	$\vec{V_7}$	$\vec{V_6}$
	$T_b = T_s \cdot \left(\frac{V_{ref}+V_{dc2}}{V_{dc2}-V_{dc1}}\right)$	(1,1,0)	(0,1,1)	(1,1,0)
VI	$T_a = -T_s \cdot \left(\frac{V_{ref}+V_{dc1}}{V_{dc2}}\right)$	$\vec{V_8}$	$\vec{V_7}$	$\vec{V_8}$
	$T_b = T_s \cdot \left(\frac{V_{dc1}+V_{dc2}+V_{ref}}{V_{dc2}}\right)$	(0,1,0)	(0,1,1)	(0,1,0)

of low THD and loss reduction are introduced and investigated. It should be noted that by proper selection of switching pattern, the minimum switching losses is achieved as follows.

In the first proposed sequence, first state vector is applied for $\frac{T_a}{2}$ of T_s, then the dwell time of T_b dedicated to second state vector and once again, the first one switches on for $\frac{T_a}{2}$. In the second proposed sequence, the duty cycle T_a is not divided and furthermore there is no symmetry in application of switching states. So, the duty cycles T_a and T_b are dedicated to first and second state vector, respectively.

As we will see, in the first proposed sequence, due to the symmetry in each sampling time period, the voltage and current waveform would have lower THD for low order harmonics than the second proposed sequence. Besides, in the first proposed sequence, due to the symmetry of switching in each sampling period, the switching frequency is higher than the second one, which results in increasing the power losses as compared to the second proposed sequence. However, it should be mentioned that both of the investigated sequences for the proposed SVM have lower THD values than the other conventional modulation techniques like level shift PWM. As mentioned before, another key point for implementation of the proposed SVM method is the normalized sampling frequency. In fact, in order to make the output pulses symmetrical during each period of the output voltage and consequently create symmetrical odd harmonics and also eliminate even harmonics at the output, the normalized sampling frequency must be a multiple of six for the seven-level inverter. In this case, the sampling periods are symmetrically distributed in six regions and consequently in the positive and negative half-cycle of the reference voltage.

Table 3 presents the duty cycle arrangements for the three-segment switching sequence method, named as first proposed sequence and shows the V_{ref} locating in all six regions. Table 4 shows the duty cycle adjustments for the two-segment switching sequence or the second proposed sequence. Note that all the switching sequences start and end in such a way that the transition of V_{ref} moving from one region to the next requires no or minimum number of switching and so, the switching sequence design requirements are satisfied.

4. Simulation Results

In this section, in order to verify the proposed simplified SVM technique on single-phase and three-phase MPUC7 inverter, MATLAB Simulink is used to survey the converter in standalone mode. The simulation parameters are shown in App. A. In order to analyze the capability of the proposed method, variation of the DC input voltage has been considered. The voltage value of the first DC source is fixed before 0.5 s and a 10 % ripple happens for the times after 0.5 s. The output seven-level voltage and current waveforms of single-

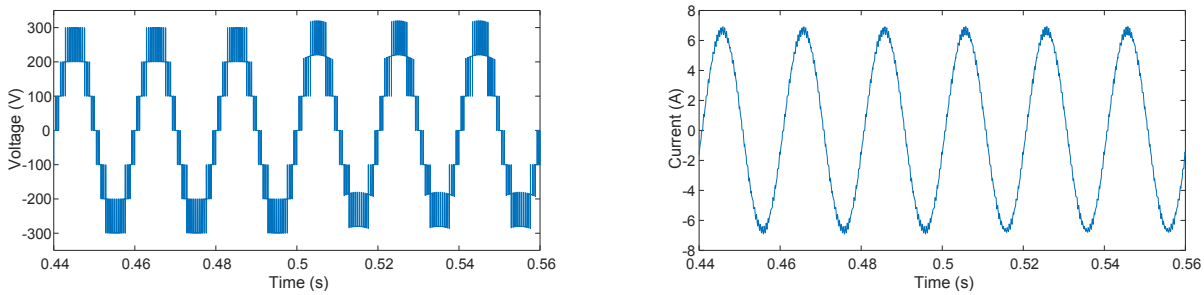
Tab. 4: Two-segment switching sequence.

Region	Situation of $\overrightarrow{V_{ref}}$	Dwell time	Switching segment 1 T_a	Switching segment 2 T_b
I	First Quadrant	$T_a = T_s \cdot \left(\frac{V_{dc1}+V_{dc2}-V_{ref}}{V_{dc2}}\right)$	$\overrightarrow{V_2}$	$\overrightarrow{V_1}$
		$T_b = T_s \cdot \left(\frac{V_{ref}-V_{dc1}}{V_{dc2}}\right)$	(1,0,0)	(1,0,1)
II		$T_a = T_s \cdot \left(\frac{V_{ref}-V_{dc1}}{V_{dc2}-V_{dc1}}\right)$	$\overrightarrow{V_3}$	$\overrightarrow{V_2}$
		$T_b = T_s \cdot \left(\frac{V_{ref}-V_{dc2}}{V_{dc1}-V_{dc2}}\right)$	(0,0,1)	(1,0,0)
III		$T_a = T_s \cdot \left(\frac{V_{dc2}-V_{ref}}{V_{dc2}}\right)$	$\overrightarrow{V_4}$	$\overrightarrow{V_3}$
		$T_b = T_s \cdot \left(\frac{V_{ref}}{V_{dc2}}\right)$	(0,0,0)	(0,0,1)
I	Second Quadrant	$T_a = T_s \cdot \left(\frac{V_{ref}-V_{dc1}}{V_{dc2}}\right)$	$\overrightarrow{V_1}$	$\overrightarrow{V_2}$
		$T_b = T_s \cdot \left(\frac{V_{dc1}+V_{dc2}-V_{ref}}{V_{dc2}}\right)$	(1,0,1)	(1,0,0)
II		$T_a = T_s \cdot \left(\frac{V_{ref}-V_{dc2}}{V_{dc1}-V_{dc2}}\right)$	$\overrightarrow{V_2}$	$\overrightarrow{V_3}$
		$T_b = T_s \cdot \left(\frac{V_{ref}-V_{dc1}}{V_{dc2}-V_{dc1}}\right)$	(1,0,0)	(0,0,1)
III		$T_a = T_s \cdot \left(\frac{V_{ref}}{V_{dc2}}\right)$	$\overrightarrow{V_3}$	$\overrightarrow{V_4}$
		$T_b = T_s \cdot \left(\frac{V_{dc2}-V_{ref}}{V_{dc2}}\right)$	(0,0,1)	(0,0,0)
IV	Third Quadrant	$T_a = T_s \cdot \left(\frac{V_{ref}+V_{dc2}}{V_{dc2}}\right)$	$\overrightarrow{V_5}$	$\overrightarrow{V_6}$
		$T_b = -T_s \cdot \left(\frac{V_{ref}}{V_{dc2}}\right)$	(1,1,1)	(1,1,0)
V		$T_a = T_s \cdot \left(\frac{V_{ref}+V_{dc1}}{V_{dc1}-V_{dc2}}\right)$	$\overrightarrow{V_6}$	$\overrightarrow{V_7}$
		$T_b = T_s \cdot \left(\frac{V_{ref}+V_{dc2}}{V_{dc2}-V_{dc1}}\right)$	(1,1,0)	(0,1,1)
VI		$T_a = T_s \cdot \left(\frac{V_{dc1}+V_{dc2}+V_{ref}}{V_{dc2}}\right)$	$\overrightarrow{V_7}$	$\overrightarrow{V_8}$
		$T_b = -T_s \cdot \left(\frac{V_{ref}+V_{dc1}}{V_{dc2}}\right)$	(0,1,1)	(0,1,0)
IV	Forth Quadrant	$T_a = -T_s \cdot \left(\frac{V_{ref}}{V_{dc2}}\right)$	$\overrightarrow{V_6}$	$\overrightarrow{V_5}$
		$T_b = T_s \cdot \left(\frac{V_{dc2}+V_{ref}}{V_{dc2}}\right)$	(1,1,0)	(1,1,1)
V		$T_a = T_s \cdot \left(\frac{V_{ref}+V_{dc2}}{V_{dc2}-V_{dc1}}\right)$	$\overrightarrow{V_7}$	$\overrightarrow{V_6}$
		$T_b = T_s \cdot \left(\frac{V_{ref}+V_{dc1}}{V_{dc1}-V_{dc2}}\right)$	(0,1,1)	(1,1,0)
VI		$T_a = -T_s \cdot \left(\frac{V_{ref}+V_{dc1}}{V_{dc2}}\right)$	$\overrightarrow{V_8}$	$\overrightarrow{V_7}$
		$T_b = T_s \cdot \left(\frac{V_{dc1}+V_{dc2}+V_{ref}}{V_{dc2}}\right)$	(0,1,0)	(0,1,1)

phase MPUC7 are depicted in Fig. 4 and Fig. 5, which have been obtained by using the first and the second switching sequence, respectively.

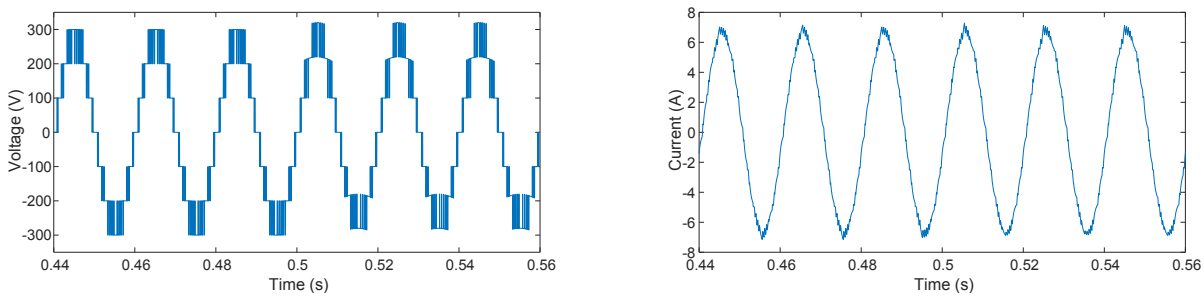
In Fig. 6, Fig. 7, Fig. 8 and Fig. 9, the THD of the output voltage and current waveforms of single-phase MPUC7 are shown for both investigated switching sequences. It should be mentioned that due to proper selection of the sampling frequency 2.1 kHz, which is normalized as a multiple of six, the output voltage pulses are distributed uniformly between positive and negative half cycles of the reference voltage signal. In this case: $F_s = 2.1$ kHz, $F_n = 50$ Hz, $m_f = 42$.

Therefore, the normalized sampling frequency has been selected as the integer multiple of number 6 ($\frac{42}{6} = 7$). So seven-level output voltage has a symmetric structure and low THD. In order to validate the performance of the proposed method for stabilizing the output voltage in case of variations in DC sources, the results are shown for fixed and variated input DC voltage cases. Evaluating the THD values shows the acceptable performance of the proposed method, which results in the small size of filter for MPUC inverter applications especially for renewable energy converter.



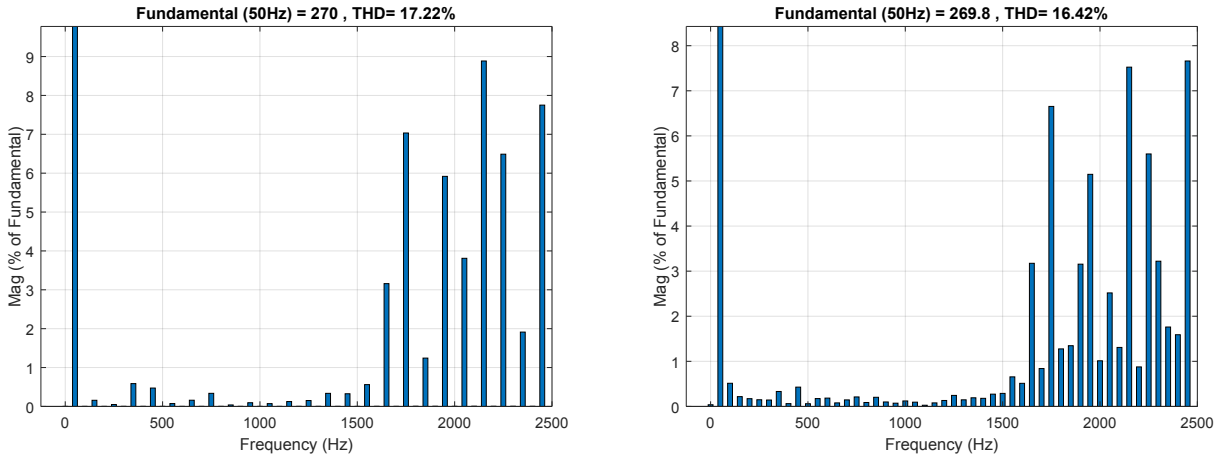
(a) Voltage. (b) Current.

Fig. 4: Voltage and current waveform at the output of single-phase MPUC7 by simplified SVM technique and using first proposed switching sequence.



(a) Voltage. (b) Current.

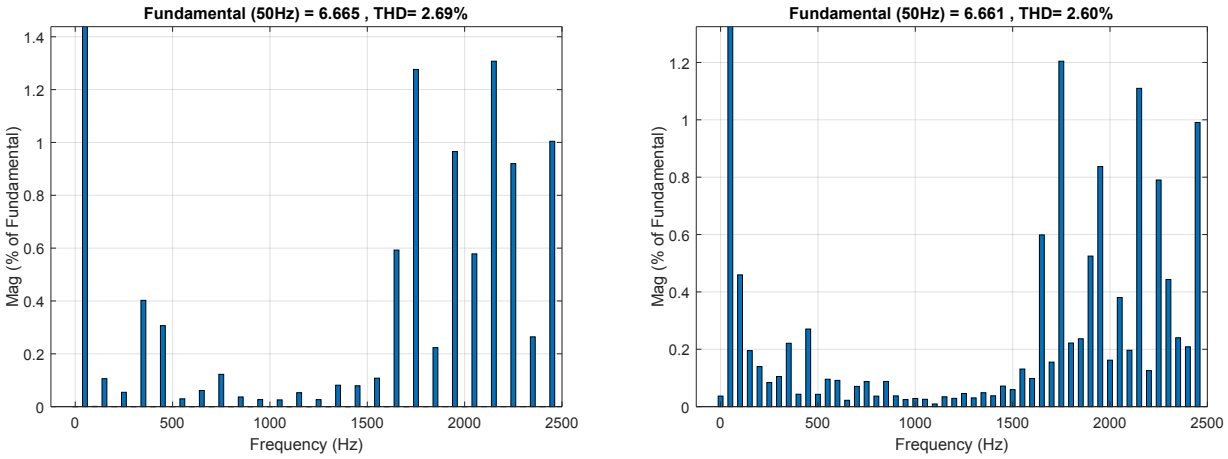
Fig. 5: Voltage and current waveform at the output of single-phase MPUC7 by simplified SVM technique and using second proposed switching sequence.



(a) Fixed input DC voltage. (b) Variable input DC voltage.

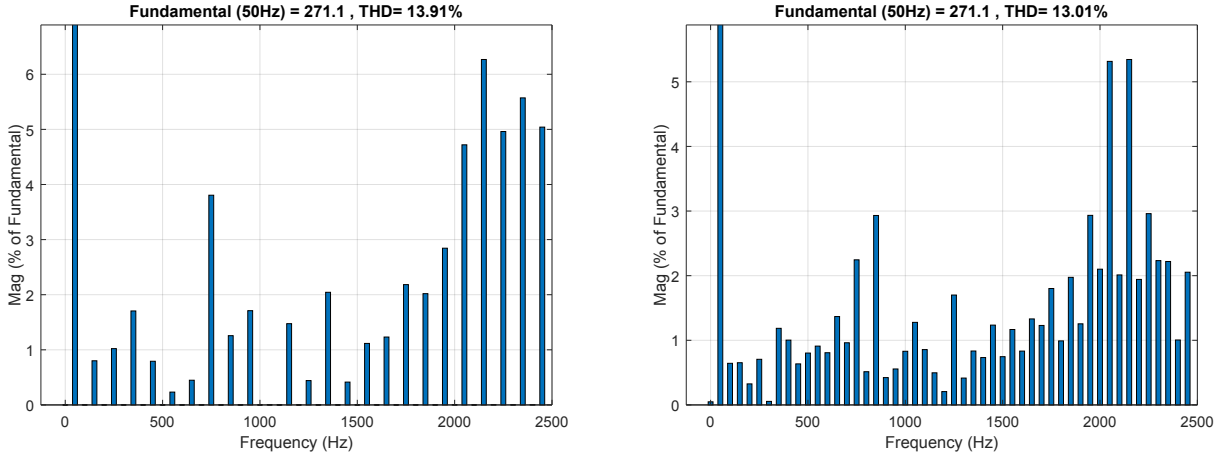
Fig. 6: FFT Analysis for output voltage by using first switching sequence.

Also, a comparison between the voltage and current THD for single-phase MPUC7 achieved by the proposed SVM technique and the LS-PWM is performed. The output voltage and current waveforms of single-phase MPUC7 obtained by LS-PWM method are depicted in Fig. 10. In Fig. 11 and Fig. 12, the THD of these waveforms are shown.The results are summarized in Tab. 5 and Tab. 6. The results from Tab. 5, show that the voltage THD achieved by the proposed method for both investigated sequences are less than LS-PWM technique. However, because of higher low-order harmonics, the current THD at second switching sequence is more than the other SVM proposed sequence and the LS-PWM technique too. The effect



(a) Fixed input DC voltage. (b) Variable input DC voltage.

Fig. 7: FFT Analysis for output current by using first switching sequence.



(a) Fixed input DC voltage. (b) Variable input DC voltage.

Fig. 8: FFT Analysis for output voltage by using second switching sequence.

of variation of input DC voltage on THD is clearly concluded from Tab. 6. As the dwell times in the proposed SVM method depends on the reference voltage amplitude and the DC input voltage, the stability of output voltage is preserved. On the other hand, the results of LS-PWM show improper voltage stability and emerging of zero and second harmonics in the output voltage and current waveforms.

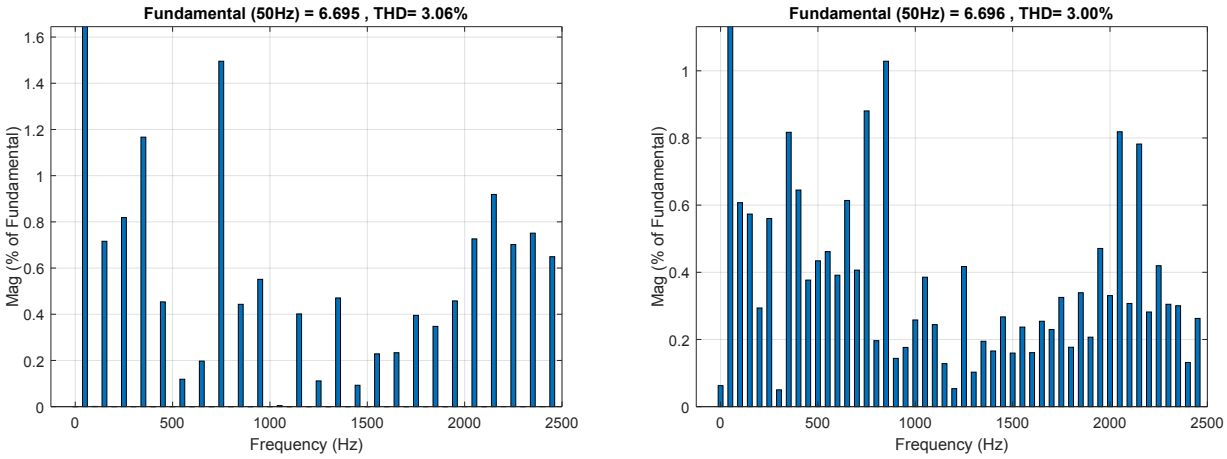
Tab. 5: Comparison among the proposed SVM switching sequences and LS-PWM for fixed input DC voltage.

THD %	First switching sequence	Second switching sequence	LS-PWM
Voltage THD	17.22	13.91	17.76
Current THD	2.69	3.06	2.79

Tab. 6: Comparison among the proposed SVM switching sequences and LS-PWM for variable input DC voltage.

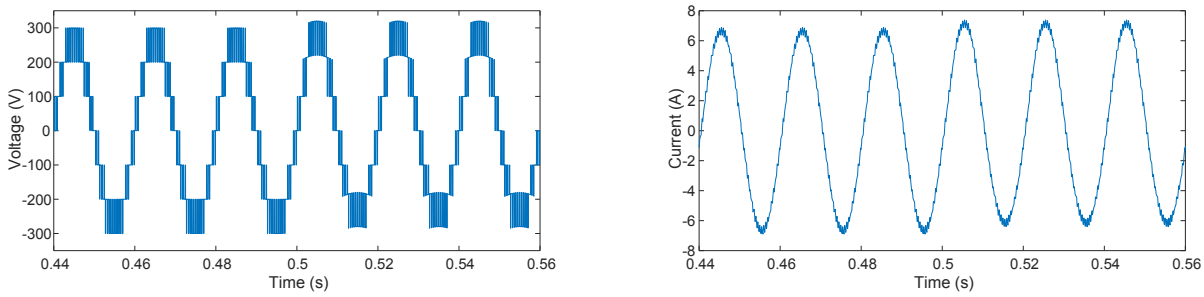
THD %	First switching sequence	Second switching sequence	LS-PWM
Voltage THD	16.42	13.01	18.29
Current THD	2.6	3	4.94

As well, Fig. 13(a) and Fig. 13(b) depict the thirteen-level line voltage waveforms, which has been obtained at the output of three-phase MPUC7 by using the first and second proposed switching sequences, respectively. As the normalized sampling frequency is multiple of six, the output pulse waveform is symmetrical and there are only odd harmonics in output voltage. By applying these proposed methods for three phase MPUC7, the 3rd order harmonics are well re-



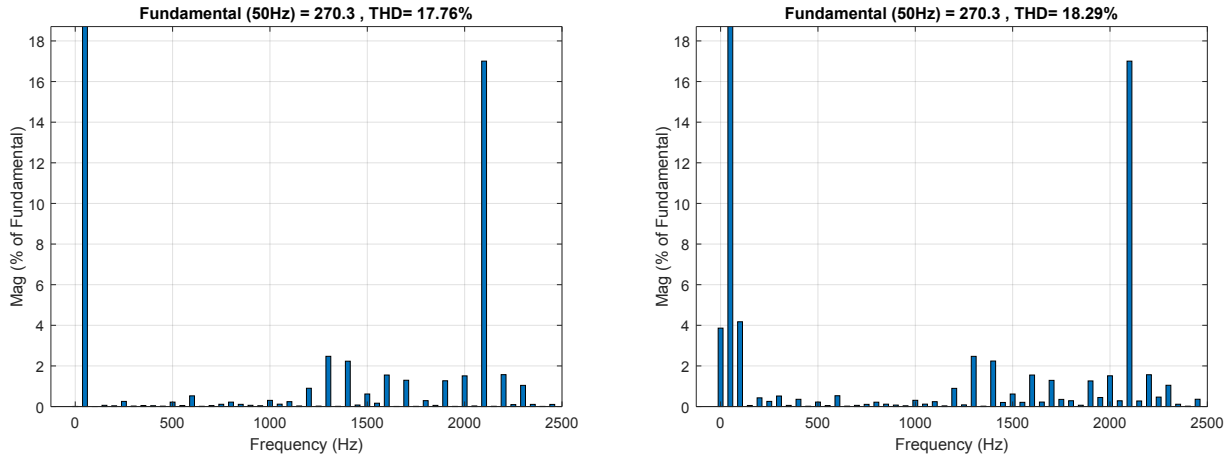
(a) Fixed input DC voltage. (b) Variable input DC voltage.

Fig. 9: FFT Analysis for output current by using second switching sequence.



(a) Voltage. (b) Current.

Fig. 10: Voltage and current waveform at the output of single-phase MPUC7 by LS-PWM method.

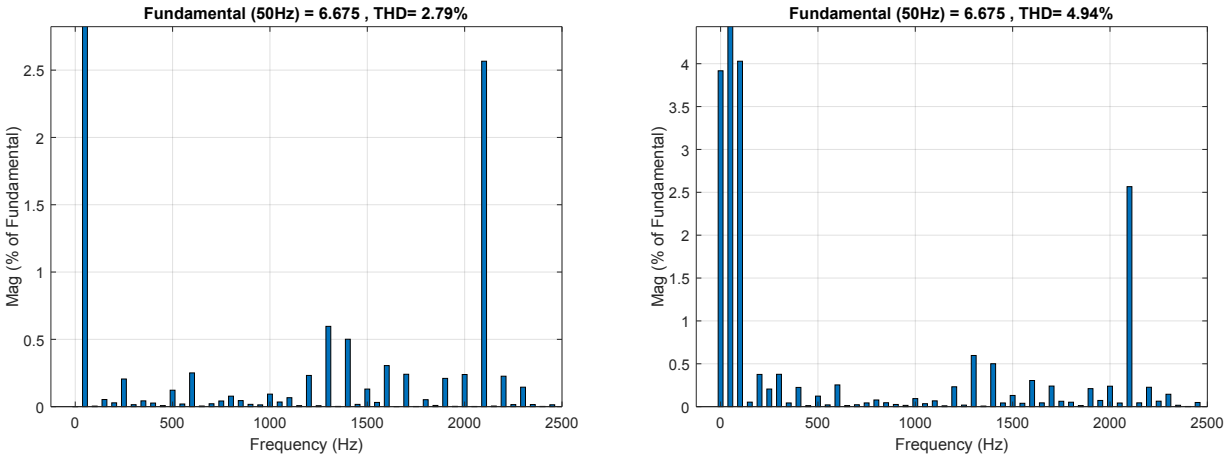


(a) Fixed input DC voltage. (b) Variable input DC voltage.

Fig. 11: FFT Analysis for output voltage by using LS-PWM method.

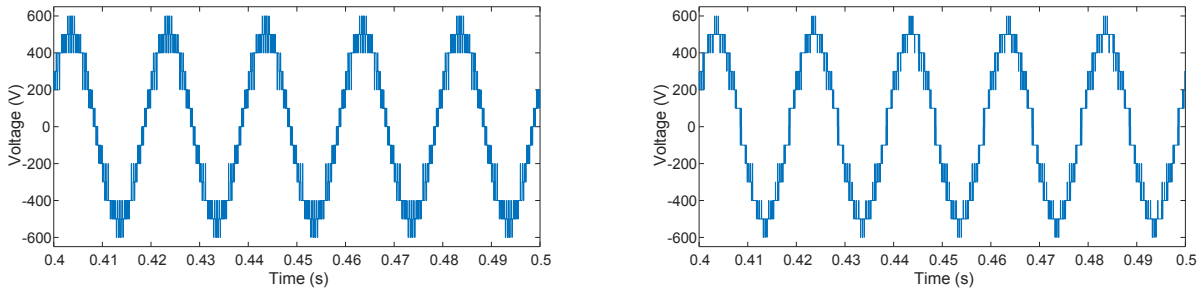
moved at the line voltage and THD is improved more, as shown in Fig. 14(a) and Fig. 14(b).

Furthermore, another case study is performed to compare the switching losses between the proposed SVM technique and LS-PWM. As can be seen



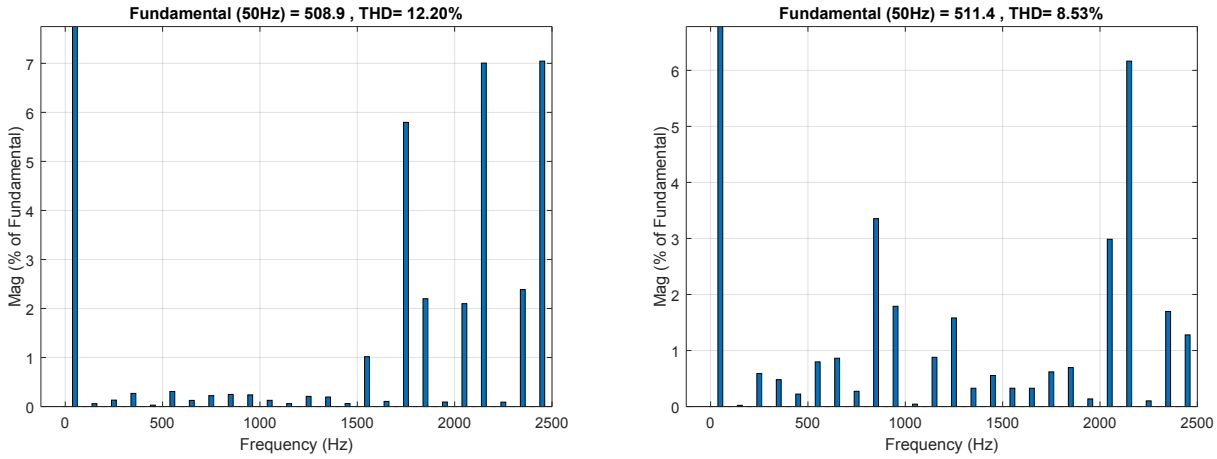
(a) Fixed input DC voltage. (b) Variable input DC voltage.

Fig. 12: FFT Analysis for output current by using LS-PWM method.



(a) First switching sequence. (b) Second switching sequence.

Fig. 13: Line voltage waveform at the output of three-phase MPUC7 by simplified SVM technique using.



(a) First switching sequence. (b) Second switching sequence.

Fig. 14: FFT Analysis for line voltage waveform at the output of three-phase MPUC7 by using.

in Fig. 15, switching patterns of switches S_1, S_2, S_3 are demonstrated for these methods for one cycle. Actually, the number of switching in each cycle, indicates the value of the switching losses of converter. The summarized results in Tab. 7, illustrate that the switching losses by applying SVM second proposed switching se-

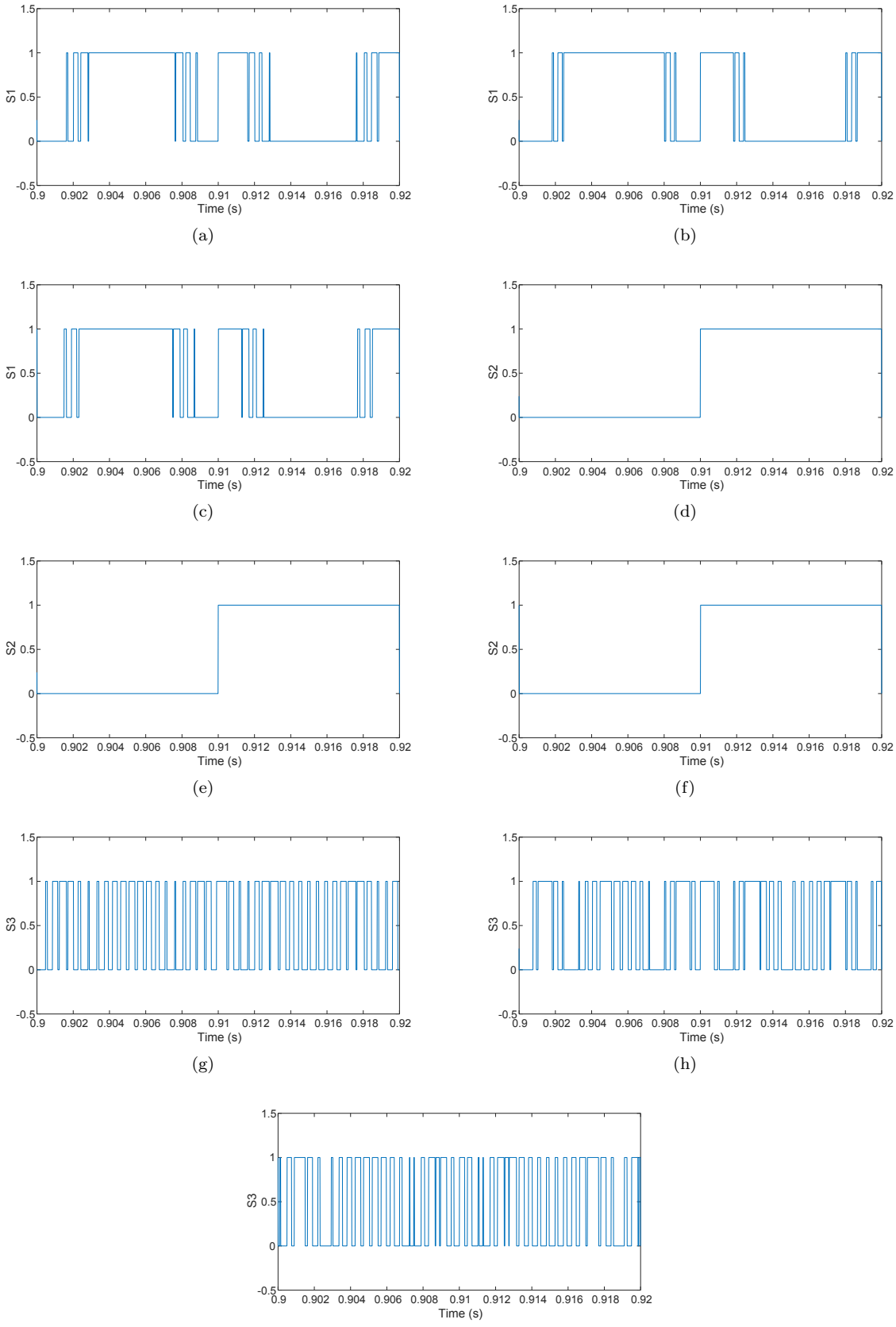


Fig. 15: Switching patterns of switches S_1, S_2, S_3 of MPUC7 for (a), (d) and (g). Proposed SVM by using first switching sequence (b), (e) and (h). Proposed SVM by using second switching sequence (c), (f) and (i) LS-PWM technique.

quence is lower than the others. Also, the total number of switching by applying the first switching sequence is equal to LS-PWM.

This simulation work can be validated through hardware implementation and the experimental setup. For building the MPUC7 converter, Six IGBT switches (600 V, 30 A, FGH30N60LSD) associated with designed snubber circuits are used. The proposed SVM method for controlling the converter needs a Digital Signal Processor (DSP)-based system for implementation. It should be noted, dSPACE products are generally compatible with all MATLAB versions. So, the designed switching patterns can be implemented on dSpace 1103 or 1104 real-time controller to generate switching pulses with proper dwell time and send associated pulses to the MPUC inverter switches. Also, Fluke 42B power analyzer is used to record THD in the output voltage and current waveform.

Tab. 7: Comparison of switching frequency between the proposed SVM switching sequences and LS-PWM.

Modulation strategy	F_s (Hz)		
	S_1	S_2	S_3
First switching sequence	15	1	41
Second switching sequence	11	1	35
LS-PWM	13	1	43

5. Conclusion

In this paper, a simplified one-dimension SVM method using two switching sequences is proposed for MPUC7 converter for single-phase and three-phase application. Then, the efficiency is evaluated by MATLAB Simulink. The MPUC7 converter can be used as the interface between solar array systems and grid. As the output DC voltage variation is a common issue in the PV system, the proposed SVM method could be implemented to minimize this effect on the MPUC7 output. Also, the proposed technique improved the THD of the voltage and current even in case of input DC voltage variation. While the analysis of the results for LS-PWM shows the inability of that technique in case of input voltage variation. Furthermore, in order to reduce the switching losses, two switching sequences were introduced. The THD value by the second sequence was better than the first sequence and LS-PWM. Besides, the power losses reduced by second sequence, significantly. Then, the proposed SVM method was applied on a three-phase MPUC7 converter and the third harmonics were well removed and the harmonic contents were improved evidently, so it can be used as a candidate to replace the conventional complex SVM methods.

Author Contributions

E.J. developed theoretical method, performed the analytic calculations and conducted modelling and numerical simulations. M.P. has contributed to modelling and simulation of the circuit. Both E.J. and M.P. authors contributed to the final version of the manuscript.

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Appendix A Simulation Parameters

- $V_1 = 200$ V,
- $V_2 = 100$ V,
- $R_{Load} = 40\ \Omega$,
- $L_{Load} = 20$ mH,
- $F_s = 2.1$ kHz,
- $m_a = 0.9$,
- $F = 50$ Hz.