# Design and Performance Analysis of High-Performance Low Power Voltage Mode Sense Amplifier for Static RAM

*Divya DUTT* [1], *Poornima MITTAL* [1], *Bhawna RAWAT* [1], *Brijesh KUMAR* [2]

[1]Department of Electronics and Communication Engineering, Delhi Technological University, Main Bawana Road, 110042 New Delhi, Delhi, India
[2]Department of Information Technology, Indira Gandhi Delhi Technical University for Women, Madrasa Road, 110006 New Delhi, Delhi, India

divyaa.dutt13@gmail.com, poornimamittal@dtu.ac.in, bhawnarawat12@gmail.com, brijeshkr@igdtuw.ac.in

DOI: 10.15598/aeee.v20i3.4373

Article history: Received Oct 04, 2021; Revised Apr 29, 2022; Accepted May 06, 2022; Published Sep 30, 2022.


***Abstract.*** *In the prominent era of the digital world and Very Large-Scale Integration (VLSI) circuits, Static Random Access Memory (SRAM) provides a vital contribution to low-power and high-speed performance. Sense Amplifiers (SA) are a part of Complementary Metal-Oxide-Semiconductor (CMOS) memories used to read the stored information. This paper indicates a Dual-Voltage, Dual-Tail Level Restoration Voltage Latch Sense Amplifier (DVDTLR-VLSA). The design has been implemented using the LT SPICE tool at* 180 *nm technology node with a* 1.8 *V supply. Performance comparison of existing SA presented in literature with the proposed SA is examined based on different parameters like power, energy, delay, and current. The proposed design maintains power at* 2.167 *μW that is decreased to half as against Dual Switch Transmission Gate Voltage SA (DTGVSA) and shows an appreciable depletion. Also, the current and delay results are improved. Dimensional analysis is also done for the proposed SA to examine the performance. After that, the effect of sleep transistors on the proposed SA examines the performance in comparison to delay and power parameters without sleep transistors. The DVDTLR-VLSA has minimal energy and power. Also, the delay is improved which may be determined more advisable for low-power operations.*

## Keywords

***Aspect ratio, average output current, bitline, energy, level restoration, sense amplifier, sleep transistor, transmission gate.***

## 1. Introduction

In the raising interest of high-speed and low-power VLSI circuits, Sense Amplifier (SA) has drawn the attention for enormous usage in CMOS memory and circuits. The SRAM circuit may explosively influence the power, delay, and stability of the design. Thus, SRAM cache is among the critical components of the modern VLSI system, and SRAM circuit is a salient element for portable electronic devices [1]. A permanent memory retains its data when power is disconnected after activation which is embedded inside "System On Chip" (SOC) circuits to provide high-level integration. SRAMs are used in consumer appliances applications since they can deeply influence the system performance concerning energy consumption, speed, and reliability [2]. It means they may perform high-speed and low-power operations. However, the major problem of SRAM circuits is the engagement of equilibrium between the writing and reading. As suggested in the literature, the cell ratio should be significant enough to permit the read access aside from changing the data [3] and [4].

SA is an essential part of the peripheral circuit for SRAM as it identifies and reads the information stored inside the bit cell during the action as far as the reading operation is completed. SA senses the bit lines' low signal voltage differences and amplifies them to the desired level, but it functions only while data is to be read in the memory. SAs are employed to amplify the low signal difference to the preferable logic level [5]. The differential SAs also called Voltage Mode SA (VMSA) are used as the static current is not passed through them. Therefore, to raise the performance and speed of memory, it is mandatory to identify and analyse various VMSAs' importance and benefits. The cross-coupled latch SAs are the most used and known due to their power and speed performance. However, it must be deliberately controlled since the input line also serves as the output line [6]. Between those SAs, the proposed SA has minimum power.

In this research work, a modified dual-voltage dual-tail level restoration voltage latch SA is designed at a 180 nm technology node that reveals low energy, delay, and power performance in comparison with any cross-coupled latch SA reported in the literature. Section 2. describes a literature review of the existing VMSA topologies. Section 3. presents the schematic design, characteristics analysis, dimensional analysis, and effect of sleep transistors on the proposed SA. A comparative analysis of the performance of the proposed SA with the pre-existing SAs is presented in Sec. 4. The findings of the paper are concluded in Sec. 5.

## 2. Existing Voltage-Mode Based SA Topologies

In this section, some well-known existing SA topologies reported in previous years are presented. The SA is a prerequisite ingredient that assembles the memory Integrated Circuit (IC) chip in the semiconductor industry. SA is the part of reading circuit systems used for data reading in the memory. Thus, it is a necessary component of functionality and performance. The SAs need reading data within the memory cells. The fundamental role of the SA is to sense the stored data based on bitline voltage discharge and to amplify the small voltage signal difference to a preferable voltage level. Thus, the stored data can be demonstrated correctly by logic aside from the memory [7]. The familiar and superior SA is SRAM based on cross-coupled voltage latch SA. Few existing SAs that achieve the desired ambition are shown in Fig. 1. The correlative property discussed in the paper for each SA is based on latch type of cross-coupled voltage mode design. W/L (Width/Length) ratio of each topology is equal i.e., 4 : 1 for all Positive channel Metal-Oxide-Semiconductor (PMOS) and 2 : 1 for NMOS transistors.

The basic High-Speed Voltage Latch SA (HSVLSA) design was reported in 2016 [8] and is shown in Fig. 1(a). In this circuit, there are three Negative channel Metal-Oxide-Semiconductor (NMOS) transistors (M3, M4, and M6) and two PMOS transistors (M1 and M2), and a CMOS inverter. The operation starts with an active Enable signal (EN), the bitline voltage differences "BL" and "BLB" are being detected by SA, and the output voltage is carried out. The suitable design of SA is the first objective for designing SRAM based circuits [9]. A CMOS inverter is attached additionally with SA output to amplify the magnitude. Due to high gain of inverter, the achieved Output (VOUT) and the cost of HSVLSA are high.

The Conventional Cross-coupled Voltage Latch SA (CCVLSA) was designed in 2019 [10] and its schematic is depicted in Fig. 1(b). Circuit consists of three sections: Driver, Access, and Load transistors. Various SAs for various memory cells are presented in literature [10]. VMSA is well-known because of its simplicity and performance. In voltage latch SA, EN needs to be selected carefully because output line also serves as input line. Footer Transistor M7 is used to bring down the leakage current during standby mode. When EN is high, then the SA conducts active mode.

The performance and current path in CCVLSA were improved by modifying it with a Double Switch Cross-coupled VMSA (DSCVMSA) [11] in 2013. For this purpose, an additional head switch and correspondent Enable (ENB) signal are introduced, as shown in Fig. 1(c). The head switch limits the weal latching transistors from being active during idle period, therefore the infirm current path is restricted, EN must be activated before ENB to transistor M1, and M3 remains to be turned "OFF". The Enable Bar signal turns "ON" the transistors M7 and M8. The output nodes charge equally to voltage of BL and BLB. When EN is active and ENB is inactive, the access transistors M7–M8 turn OFF. Then, node at the source of head switch M1 is picked up to Vdd and node at drain of bottom switch M6 takes out to the ground level. Thus, the output towards BL will be identical to power supply (Vdd) and output towards BLB will be equal to zero. This demonstrates that stored data in BL is 1 and stored data in BLB is 0.

A nine transistor Conventional Latched SA [12] is illustrated in Fig. 1(d). Here, transistors M2, M3, M5 and M6 form cross-coupled inverter. When EN is "1", PMOS transistors M8 and M9 are used for decoupling. M1 is precharge to supply voltage [8]. In CLSA, EN signal must be direct attentively due to difference in voltage between drain and source of PMOS M9 and

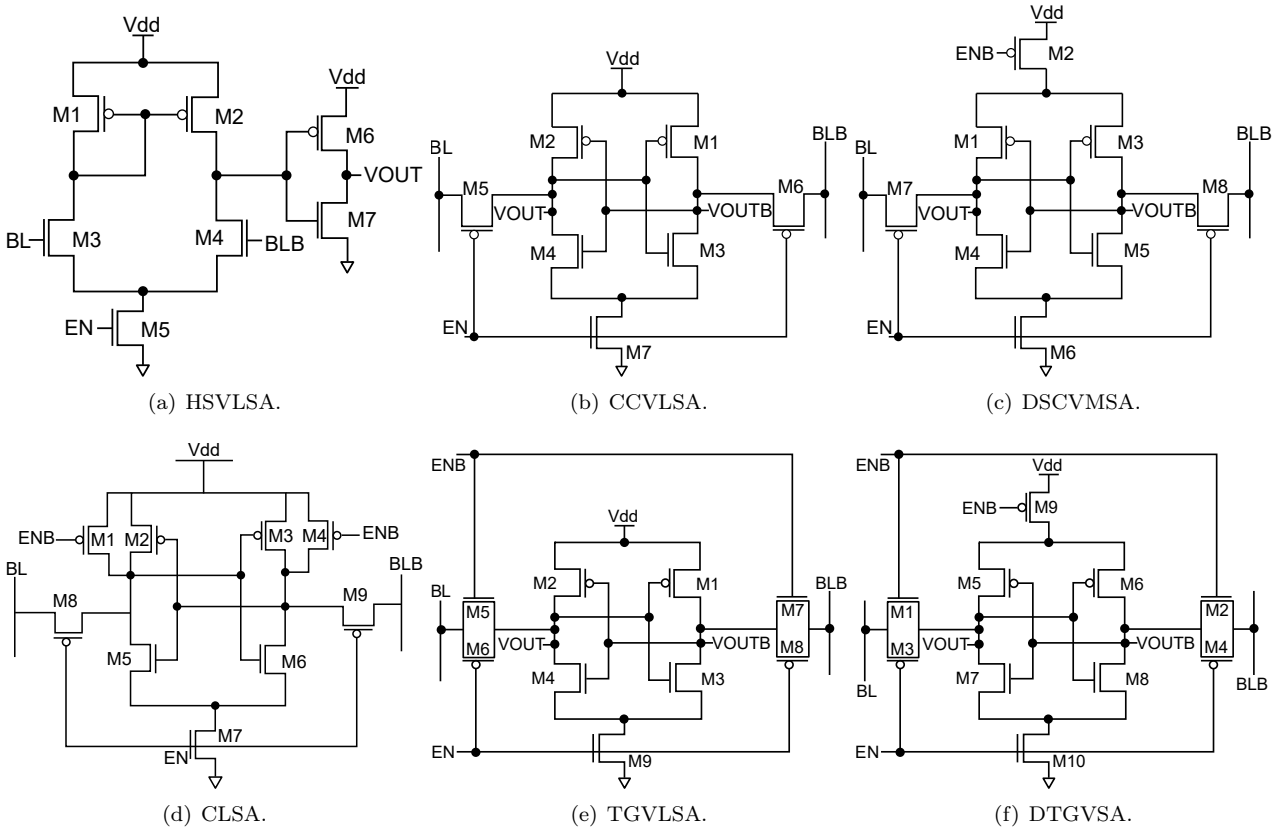



**Fig. 1:** Circuit diversity.

M8, and leakage of current flow from output node to bit lines.

The design for Transmission Gate Voltage Latch SA (TGVLSA) was reported in 2019 [10] and its schematic is depicted in Fig. 1(e). The design consists of four PMOS (M6, M8, M1 and M2) and five NMOS (M3, M4, M5, M7 and M9) transistors. TGVLSA works in the same way as CCVLSA, only two additional transistors M5 and M7 are added by two PMOS transistors M6 and M8 which form a transmission gate. The transmission gate transistors are attached to BLB and BL. The delay and power of TGVLSA are improved as compared to CCVLSA. Therefore, transmission gate is the combination of PMOS and NMOS also known as analog or CMOS switch. TGVLSA is used to allow or reject a signal towards output [13] and [14]. The transmission gate is used to control gate signal and acts as a bi-directional switch.

The Dual switch Transmission Gate Voltage latch SA (DTG-VSA) [11] was designed to depreciate the power consumption and remove the leakage current is depicted in Fig. 1(f). The head switch transistor M10 and foot switch transistor M10 relates to enable EN respectively in the SA to avoid leakage current. Sleep switches are used to decrease leakage current [15]. The SA comprises of five PMOS and four NMOS transistors where transistors M5–M8 are used to make inverter circuit and transistors M3 and M4 are access transistors. When EN is "high" and ENB is "low", the sleep transistors M9 and M10 are turned "ON". Assuming BL is "high" and BLB is "low". When EN is equal to 0 and ENB is 1, M9 and M10 gets turned "OFF" and transmission gate transistors (M1, M3, M4, M2) will be turned "ON". By this, output node charges BL and BLB equally. Due to dual switch and decreased leakage current, the energy is falling off and the speed is expanded.

## 3. Schematic Diversity and Parameter Extraction of the Proposed Sense Amplifier

Differential Sense Amplifiers are used as the static current is not passed through them which will help in reducing power. Also, they are authentic. The main liability of SA is to detect the stored data of bitline voltage discharge. However, differential SA uses most silicon area. Therefore, high packing density is required. A Level Restoration Circuit (LRC) sets out a voltage swing from "0" to "1" logic level. LRCs can be used in VLSI Metal-Oxide-Semiconductor (MOS)

digital circuit designs. In Fig.2, primary level restoration circuit along with pass transistor is presented [16]. LR circuits are normally brought in because of their authenticity and also have low short circuit dissipation due to positive feedback transistor (M2).

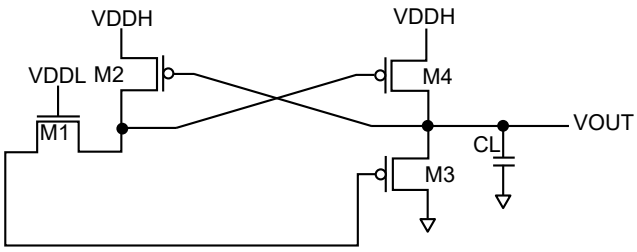



**Fig. 2:** Primary level restoration circuit along pass transistor.

## 3.1. Schematic Design of the Proposed Circuit

A Dual-Voltage Dual-Tail Level Restoration Voltage Latch Sense Amplifier (DVDTLR-VLSA) including two sleep transistors is reported in the paper. The schematic design of the proposed SA consists of ten transistors, as depicted in Fig. 3. The circuit design of the proposed SA is the same as double switch cross coupled VMSA [11], only two additional PMOS transistors M1 and M2 are attached. Also, there are two divisions of circuit connected to Vdd. The DVDTLR-VLSA amplifies the bitline voltage difference ΔVBLB and ΔVBL.

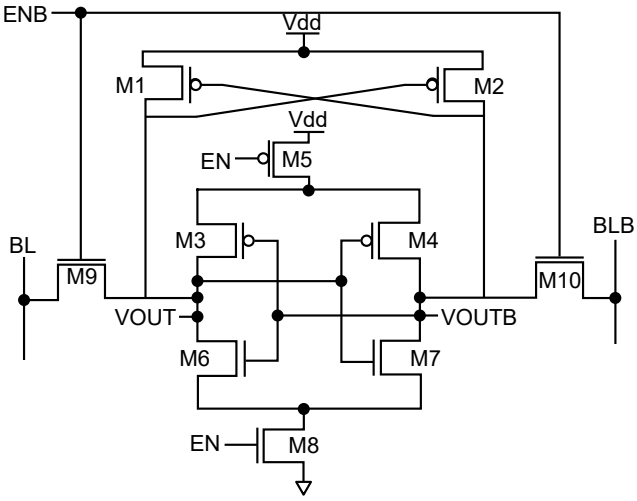



**Fig. 3:** Schematic diagram of the proposed SA.

Level restoration circuits are used in MOS logic designs as they supply low-to-high valid logic level of voltage swing in reaction to a low swing input signal Dual voltage with swing restoration logic is used [16]. When EN is "1" and ENB is "0", the enabling transistors M8 and M5 are turned "ON". Assuming (BLB = "0") and (BL = "1"), while ENB = 1, EN = 0, and sleeping transistor gets turned "OFF". This will charge output nodes.

## 3.2. Performance Analysis of the Proposed SA

In this section, the simulated results of the proposed SA are examined. All the simulations have been performed using LT SPICE tool. In Fig. 4(a), output functionality of the proposed SA is presented. When EN signal and BL are high, then output $V(p)$ follows the BL. Similarly, when ENB is active low and BL is high, the output $V(q)$ acts in accordance with BLB. By this waveform, working of SA can be confirmed. In Fig. 4(b) and Fig. 4(c), power and current waveforms are presented respectively.

Power is a critical parameter nowadays. The low power is important to avoid supplementary system required for cooling which can cause a portable problem [17] and [18]. Thus, cost of the systems raises due to additive system.

## 3.3. Dimensional Analysis of the Proposed SA

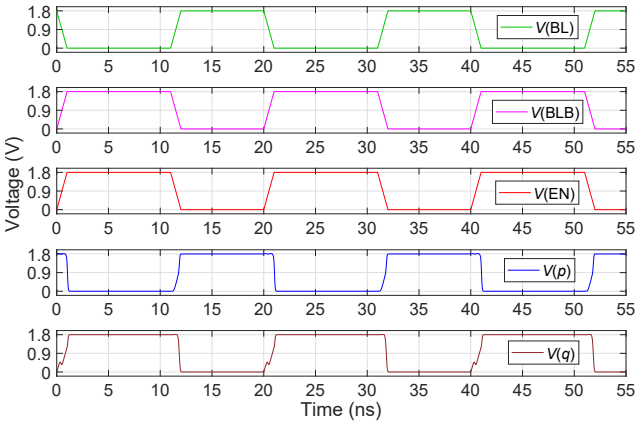
Speed performance of any SA can be recognized by knowing how fast the output nodes become charged. Therefore, correct designing is necessary to charge output nodes through precharge transistors in minimum time.

In Fig. 5, the aspect ratio of driver transistors and load transistors is arranged to attain perfect pull-up ratio and cell ratio [19]. Length of all driver and load transistors is 180 nm, while the widths ($w$) of transistors M3, M4, M6 and M7 are 900 nm, 900 nm, 300 nm and 300 nm respectively.

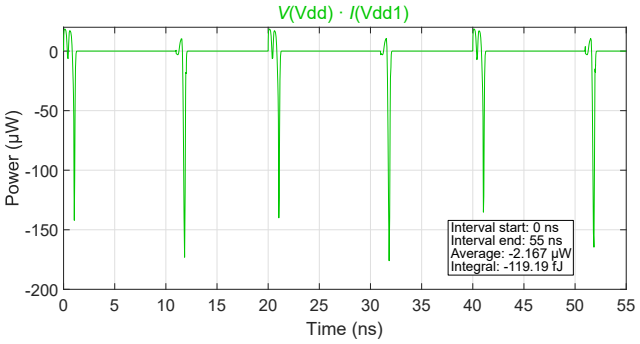
The design is analysed for low-power, low-energy, and satisfactory speed operation. The proposed SA is designed to store and amplify low voltage difference between the bitlines to yield desired logic level and also to reduce time for charging the output node. It can be surmised from Fig. 6(a) and Fig. 6(b) that when the aspect ratios of driver and load transistor are 900/180 nm and 300/180 nm, the best output results are achieved by this ratio as the output node charges fast. By this method, the speed of SA can be improved.

## 3.4. Sleep Transistor Effect on the Proposed SA

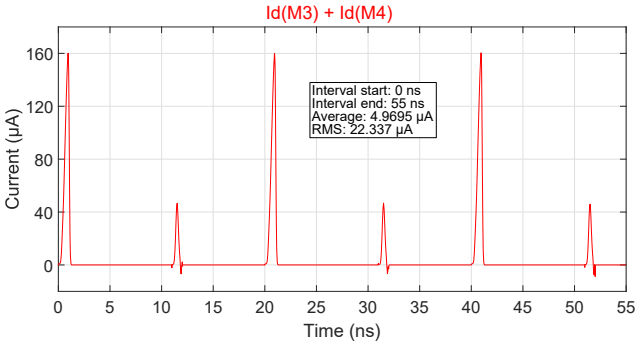
One among the low-power techniques used for VLSI circuits is power gating. It is used to save the power




(a) Functionality analysis.




(b) Power analysis.




(c) Current analysis.

**Fig. 4:** Output analysis of SA.

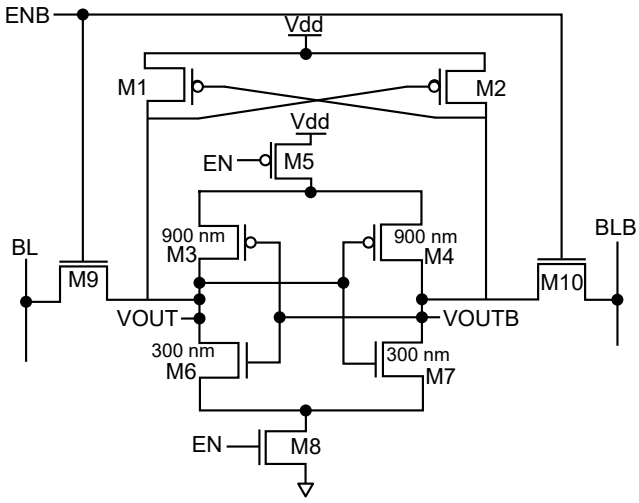
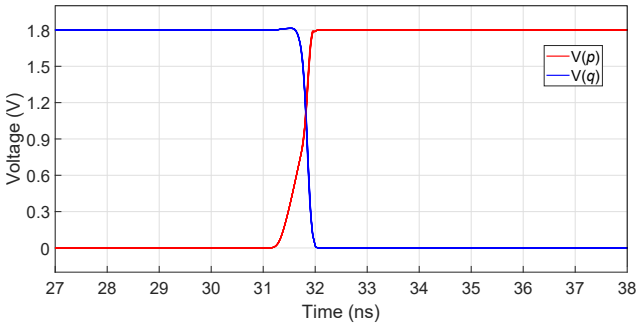
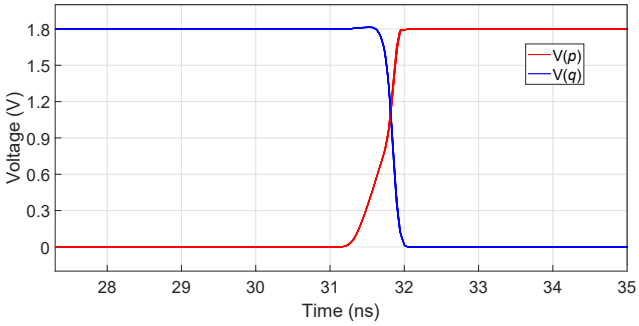



**Fig. 5:** Schematic of the proposed SA with labelled aspect ratios.




(a) PMOS $w = 900$ nm.




(b) NMOS $w = 300$ nm.

**Fig. 6:** Output waveform with various width.

by turning off the switch of the unused portion of circuit. PMOS and NMOS transistors are used as power switches. Another name for power switches is sleep transistors. NMOS and PMOS are used as power supply rails Vss and Vdd, respectively.

The impact of sleep transistor on the SRAM is reported by researchers in reference [20]. In Fig. 7, the bottom sleep transistor is removed from the proposed SA. After removing bottom sleep transistor, we get power and delay of 3.7 µW and 256.78 ps, respectively. Table 1 shows the result comparison of SA with or without sleep transistor.

**Tab. 1:** Effect of sleep transistor.

| | **Power (µW)** | **Delay (ps)** |
|---|---|---|
| **Proposed SA** | 2.16 | 262.03 |
| **Proposed SA without sleep transistor** | 3.70 | 256.78 |

It is shown in Tab. 1 that SA with sleep transistor is consuming lower power i.e., 2.16 µW than that of SA without sleep transistors i.e., 3.7 µW while there is not too much variation in delay results. It is due to reduction of leakage. The NMOS transistor is at-

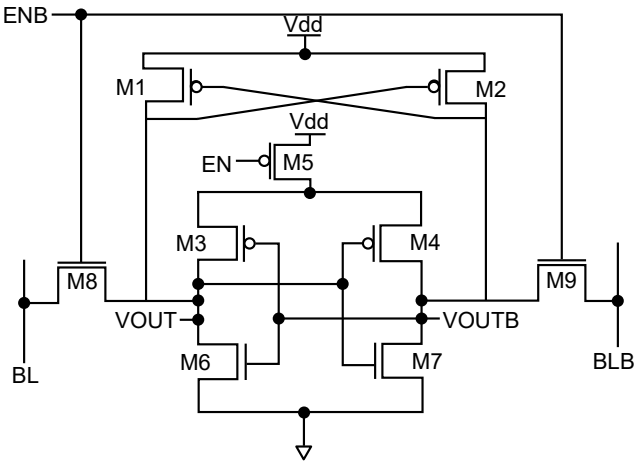



**Fig. 7:** Proposed SA without bottom sleep transistor.

tached to circuit and ground. Hence, it is called footer transistor.

# 4. Performance Comparison of Existing SA with the Proposed SA

Comparative performance analysis of various cross coupled voltage mode SAs with the proposed SA is presented in this section. The four main designs aimed in the VLSI industry are speed, delay, power, and area. Paper is summed up based on the design extent to analyze the stability within these parameters [20] and [21]. Low power is necessary for portable devices [22].

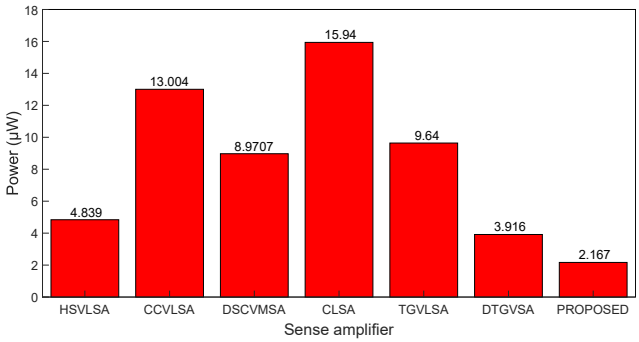
## 4.1. Energy and Power Performance

Power consumption is a principal parameter of entire VLSI circuits. With the rising request for low power circuits, research on lowering power consumption for SA is getting popular [23]. It may be surmised from Fig. 8(a) that among existing SAs, DVDTLR-VLSA has the low energy as well as the lowest power. Comparative energy analysis is shown in Fig. 8(b). The product of delay and power also known as switching energy is used to calculate the energy. Here, Power $P = V \cdot I$.

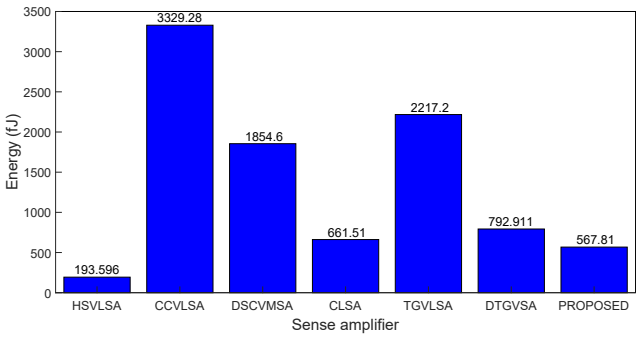
## 4.2. Delay Analysis

As the interest of high-speed circuit increases, delay factor becomes more important in VLSI circuits [24].

It can be surmised from Fig. 9 that SA i.e., HSVLSA has the lowest delay and therefore, it is the best choice. Also, there is a tradeoff between other topologies pre-




(a) Analytical output waveform of comparative power.




(b) Analytical output waveform of comparative energy.

**Fig. 8:** Analytical output waveform of (a) comparative power and (b) comparative energy.

sented in Tab. 2. Propagation delay of logic circuit is defined as time needed for output voltage to hold out the midway between the 0 and 1 logic levels. i.e., half (50 %) of Vdd:

$$\tau_p = \frac{\tau_{phl} + \tau_{plh}}{2}, \tag{1}$$

where $\tau_p$, $\tau_{phl}$ and $\tau_{plh}$ are known as total propagation delay, high-to-low transition delay and low-to-high transition delay, respectively. Results are obtained by assuming aspect ratios of PMOS's of 4 : 1 and NMOS's of 2 : 1.

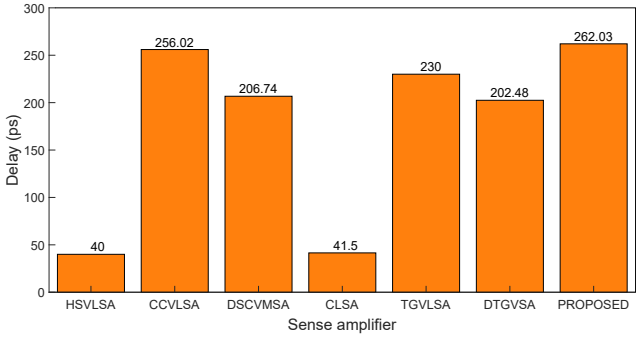



**Fig. 9:** Delay comparison.

**Tab. 2:** Comparison of SA configuration designed at 180 nm technology node and evaluated for 1.8 V supply [10].

| Sense amplifiers with power supply 1.8 V | Power (µW) | Energy (fJ) | Delay (ps) | Average current (µA) | Number of transistors |
|---|---|---|---|---|---|
| **HSVLSA** | 4.839 | **193.596** | **40** | 0.412 | 7 |
| **CCVLSA** | 13.004 | 3329.28 | 256.02 | 0.796 | 7 |
| **DSCVMSA** | 8.9707 | 1854.60 | 206.74 | 0.514 | 8 |
| **CLSA** | 15.94 | 661.51 | 41.50 | 2.230 | 9 |
| **TGVLSA** | 9.64 | 2217.2 | 230.00 | 2.504 | 9 |
| **DTGVSA** | 3.916 | 792.911 | 202.48 | 2.229 | 10 |
| **Proposed SA** | **2.167** | 567.81 | 262.03 | **4.878** | 10 |

### 4.3. Comparative Current Analysis

In Fig. 10, comparative results of current of all SA topologies are presented. Current ($I$) equals to power divided by voltage ($I = P \cdot V^{-1}$). Here we have calculated the average current passing towards the output nodes.

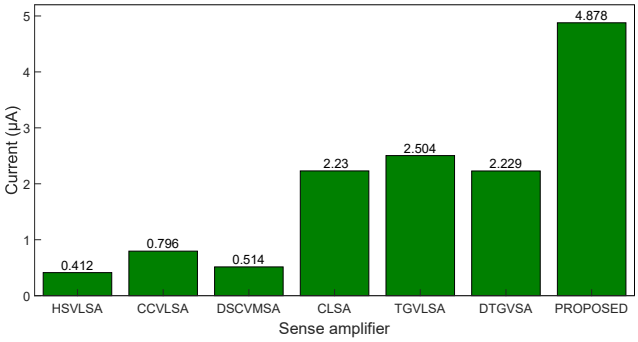



**Fig. 10:** Current analysis.

It can be surmised from the Fig. 10 that HSVLSA has the lowest current and DVDTLR-VLSA possesses the maximum current i.e., 4.878 µA. It is because of transistor count and dual voltage present. Current of the proposed design is high, but consuming lowest power. The comparative data of parameters; power, switching energy delay and current of each SA evaluated for 1.8 V is given in Tab. 2 [25].

## 5. Conclusion

This paper has decorated performance upgradation of Sense Amplifier (SA) and a dual-voltage dual-tail level restoration voltage latch SA (DVDTLR-VLSA) has been reported. The SA is designed at a 180 nm technology node and 1.8 V power supply. Comparative Transient analysis for each SA with the proposed SA is done at 55 ns pulse width. The DVDTLR-VLSA is modified mainly for high-speed and low-power consequences. It can be inferred from the simulated results that the power of the modified SA is the lowest, specifically 2.2 µW. That is notably improved compared to existing SAs analysed in the paper. Two additional analyses have been done for DVDTLR-VLSA which show the proposed design to be the best case. As in the case of SA without sleep transistors, the power is increased. The DVDTLR-VLSA is designed for low-power circuits.

## Author Contributions

D.D. and P.M. conceived the idea and planned the complete work. D.D. and B.R. has carried out all the simulations and plotted/analysed all the results. D.D. and P.M. performed the calculations and analysed the data for interpretation of the results and graph modification. P.M. and B.K. designed the model and the computational framework. D.D. and B.R. drafted first write-up of the manuscript. B.R., P.M. and B.K. prepared the revised manuscripts and prepared the detailed response to the reviewer comments. All the authors provided critical feedback and helped shape the research, analysis and manuscript.

## References

[1] RAWAT, B. and P. MITTAL. Single bit line accessed high-performance ultra-low voltage operating 7T static random access memory cell with improved read stability. *International Journal of Circuit Theory and Applications*. 2021, vol. 49, iss. 5, pp. 1435–1449. ISSN 1097-007X. DOI: 10.1002/cta.2960.

[2] ZHU, J., N. BAI. and J. WU. A Review of Sense Amplifiers for Static Random Access Memory. *IETE Technical Review*. 2013, vol. 30, iss. 1, pp. 72–81. ISSN 0974-5971. DOI: 10.4103/0256-4602.107343.

[3] NEGI, S., P. MITTAL and B. KUMAR. Modeling and Analysis of High-Performance Triple Hole Block Layer Organic LED Based Light Sensor for Detection of Ovarian Cancer. *IEEE Transactions on Circuits and Systems I: Regular Papers*. 2021, vol. 68, iss. 8, pp. 3254–3264. ISSN 1558-0806. DOI: 10.1109/TCSI.2021.3078510.

[4] GARG, M. R. and A. TONK. A Study of Different Types of Voltage & Current Sense Amplifiers used in SRAM. *International Journal of Advanced Research in Computer and Communication Engineering*. 2015, vol. 4, iss. 5, pp. 30–35. ISSN 2278-1021. DOI: 10.17148/IJARCCE.2015.4507.

[5] KOBAYASHI, T., K. NOGAMI, T. SHIROTORI and Y. FUJIMOTO. A current-controlled latch sense amplifier and a static power-saving input buffer for low-power architecture. *IEEE Journal of Solid-State Circuits*. 1993, vol. 28, iss. 4, pp. 523–527. ISSN 1558-173X. DOI: 10.1109/4.210039.

[6] JAIN, R., K. GUPTA. and N. PANDEY. Hybrid Dynamic CML with Modified Current Source (H-MDyCML): A Low-Power Dynamic MCML Style. *Advances in Electrical and Electronic Engineering*. 2021, vol. 19, iss. 1, pp. 57–65. ISSN 1804-3119. DOI: 10.15598/aeee.v19i1.3944.

[7] RAWAT, B. and P. MITTAL. A 32 nm single-ended single-port 7T static random access memory for low power utilization. *Semiconductor Science and Technology*. 2021, vol. 36, iss. 9, pp. 6–22. ISSN 1361-6641. DOI: 10.1088/1361-6641/ac07c8.

[8] PATHRIKAR, A. K. and R. S. DESHPANDE. Design of faster & power efficient sense amplifier using VLSI technology. In: *2016 IEEE International Conference on Advances in Electronics, Communication and Computer Technology (ICAECCT)*. Pune: IEEE, 2016, pp. 358–361. ISBN 978-1-5090-3662-2. DOI: 10.1109/ICAECCT.2016.7942613.

[9] CHRISANTHOPOULOS, A., Y. MOISIADIS, Y. TSIATOUHAS and A. ARAPOYANNI. Comparative study of different current mode sense amplifiers in submicron CMOS technology. *IEE Proceedings - Circuits, Devices and Systems*. 2002, vol. 149, iss. 3, pp. 154–158. ISSN 1359-7000. DOI: 10.1049/ip-cds:20020425.

[10] KISHORE, C. and A. KUMAR. Comparative Analysis of Various Sense Amplifiers in 45nm CMOS Technology. *International Research Journal of Engineering and Technology*. 2019, vol. 6, iss. 5, pp. 102–106. ISSN 2395-0056.

[11] NA, T., S.-H. WOO, J. KIM, H. JEONG and S.-O. JUNG. Comparative Study of Various Latch-Type Sense Amplifiers. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*. 2014, vol. 22, iss. 2, pp. 425–429. ISSN 1557-9999. DOI: 10.1109/TVLSI.2013.2239320.

[12] GUNDU, A. K., M. S. HASHMI and A. GROVER. A New Sense Amplifier Topology with Improved Performance for High Speed SRAM Applications. In: *2016 29th International Conference on VLSI Design and 2016 15th International Conference on Embedded Systems (VLSID)*. Kolkata: IEEE, 2016, pp. 185–190. ISBN 978-1-4673-8700-2. DOI: 10.1109/VLSID.2016.38.

[13] KUMAR, N., P. MITTAL and M. MITTAL. Performance Analysis of FinFET based 2:1 Multiplexers for Low Power Application. In: *2020 IEEE Students Conference on Engineering & Systems (SCES)*. Prayagraj: IEEE, 2020, pp. 1–5. ISBN 978-1-7281-9339-7. DOI: 10.1109/SCES50439.2020.9236770.

[14] ETEZADI, S. and S. A. HOSSEINI. Novel Ternary Logic Gates Design in Nanoelectronics. *Advances in Electrical and Electronic Engineering*. 2019, vol. 17, iss. 3, pp. 294–305. ISSN 1804-3119. DOI: 10.15598/aeee.v17i3.3156.

[15] KUMAR, N., P. MITTAL, B. RAWAT and M. MITTAL. Dynamic Power Consumption and Delay Analysis for Ultra-Low Power 2 to 1 Multiplexer Designs. *Advances in Electrical and Electronic Engineering*. 2021, vol. 19, iss. 2, pp. 145–154. ISSN 1804-3119. DOI: 10.15598/aeee.v19i2.3821.

[16] MOISIADIS, Y., I. BOURAS and A. ARAPOYANNI. High performance level restoration circuits for low-power reduced-swing interconnect schemes. In: *7th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*. Jounieh: IEEE, 2000, pp. 619–622. ISBN 0-7803-6542-9. DOI: 10.1109/ICECS.2000.911615.

[17] PAL, P. K. and R. K. NAGARIA. A Low Power Low Supply MOS-Only Subthreshold Voltage Reference for Wide Temperature Range. *Advances in Electrical and Electronic Engineering*. 2019, vol. 17, iss. 2, pp. 167–178. ISSN 1804-3119. DOI: 10.15598/aeee.v17i2.3197.

[18] RATHOD, A. P. S., P. LAKHERA, A. K. BALIGA, P. MITTAL and B. KUMAR. Performance comparison of pass transistor and CMOS logic configuration based de-multiplexers. In: *International Conference on Computing, Communication & Automation*. Greater Noida: IEEE, 2015, pp. 1433–1437. ISBN 978-1-4799-8890-7. DOI: 10.1109/CCAA.2015.7148606.

[19] KANIKA and P. K. DAHIYA. Analyzing the Impact of Sleep Transistor on SRAM. *IOSR Journal of VLSI and Signal Processing*. 2017, vol. 7, iss. 3, pp. 64–67. ISSN 2319-4200. DOI: 10.9790/4200-0703016467.

[20] GOYAL, A., A. TOMAR, and A. GOYAL. Effect of W/L Ratio on SRAM Cell SNM for High-

Speed Application. *International Research Journal of Engineering and Technology*. 2017, vol. 4, iss. 4, pp. 2326–2332. ISSN 2395-0056.

[21] YANG, B.-D. and L.-S. KIM. A low-power SRAM using hierarchical bit line and local sense amplifiers. *IEEE Journal of Solid-State Circuits*. 2005, vol. 40, iss. 6, pp. 1366–1376. ISSN 1558-173X. DOI: 10.1109/JSSC.2005.848032.

[22] SHARMA, V., S. COSEMANS, M. ASHOUEI, J. HUISKEN, F. CATTHOOR and W. DEHAENE. A 4.4 pJ/Access 80 MHz, 128 kbit Variability Resilient SRAM With Multi-Sized Sense Amplifier Redundancy. *IEEE Journal of Solid-State Circuits*. 2011, vol. 46, iss. 10, pp. 2416–2430. ISSN 1558-173X. DOI: 10.1109/JSSC.2011.2159056.

[23] SEEVINCK, E., P. J. VAN BEERS and H. ONTROP. Current-mode techniques for high-speed VLSI circuits with application to current sense amplifier for CMOS SRAM's. *IEEE Journal of Solid-State Circuits*. 1991, vol. 26, iss. 4, pp. 525–536. ISSN 1558-173X. DOI: 10.1109/4.75050.

[24] BLALOCK, T. N. and R. C. JAEGER. A high-speed clamped bit-line current-mode sense amplifier. *IEEE Journal of Solid-State Circuits*. 1991, vol. 26, iss. 4, pp. 542–548. ISSN 1558-173X. DOI: 10.1109/4.75052.

[25] KHELLAH, M. M. and M. I. ELMASRY. A low-power high-performance current-mode multiport SRAM. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*. 2001, vol. 9, iss. 5, pp. 590–598. ISSN 1557-9999. DOI: 10.1109/92.953493.

## About Authors

**Divya DUTT** was born in Delhi, India in 1997. She received her B.Tech. degree in Electronics and Communication Engineering from Raj Kumar Goel Institute of Technology, Ghaziabad, India in 2019. She received her M.Tech. degree from Delhi Technological University, New Delhi, India. Her research interests include Low Power VLSI Circuits, Amplifier Circuits.

**Poornima MITTAL** (IEEE member) has published 10+ international journal/conference papers/book chapters. Her research interest includes design/modelling of flexible electronic devices, material synthesis and characterization, electronic and optical materials, thin film fabrication, Organic Light-Emitting Diode (OLED), solar cell, memory design and low power VLSI circuits. She has published one patent on novel Organic Thin-Film Transistor structure and textbook titled "Organic Thin-Film-Transistor Applications: Materials to Circuits", CRC Press, United Kingdom, 2016. She is the reviewer of many IEEE transactions and other international journals of IEEE, Elsevier, Springer, IOP, AVS, Wiley and T&F. She has received the research awards in 2012 and 2015 for dedicated research at Graphic Era University, Dehradun, India. Also, she has received Commendable- Research-Award in 2019, 2020, 2021 and 2022 at Delhi Technological University (DTU), Delhi, India. She is the life member of many professional societies. She has more than 15 years of academic and research experience and presently, she is working as professor in the department of Electronics and Communication Engineering at DTU, Delhi, India.

**Bhawna RAWAT** was born in Delhi, India in 1993. She received her B.Tech. degree in Electronics and Communication Engineering from Shiv Nadar University, Greater Noida, India in 2015. She received M.Tech. degree in VLSI Design from Indira Gandhi Delhi Technical University for Women, Delhi, India. She is presently pursuing Ph.D. at Delhi Technological University, New Delhi, India. Her research interests include low power circuit design, memory circuits in emerging technologies.

**Brijesh KUMAR** is presently working as a professor in the Department of Information Technology, Indira Gandhi Delhi Technical University for Women, Delhi, India since April 2022. Prof. Kumar earned a B.Tech. degree at Bundelkhand Institute Engineering and Technology (B.I.E.T.), Jhansi (Uttar Pradesh) India; and M.Tech. at Dr. A.P.J. Abdul Kalam Technical University, Lucknow, India; and a Ph.D. at Indian Institute of Technology (IIT), Roorkee, India. He has more than 150 international, national journals and conference publications, patents, book, book chapter publications as well. His research interest includes Internet of Things (IoT) Based Smart Devices and Testing, Artificial Intelligence and Machine Learning Applications, Data Communication and Computer Network, Memory Designs, Flexible Electronics, Electronic Devices and Circuits, VLSI Design and Technology, Digital System Design, Semiconductor Novel Device Structures.