Neoteric Design Power Sustained 3-Bit Asynchronous Counter Using CNFET Based MCML Topology

Ramsha SUHAIL [1] , Pragya SRIVASTAVA [1] , Richa YADAV [1] , Richa SRIVASTAVA [2]

[1] Department of Electronics and Communication Engineering, Indira Gandhi Delhi Technical University for Women, Madrasa Road, Opposite St. James Church, Kashmere Gate, 110006 New Delhi, Delhi, India
[2] Department of Electronics and Communication Engineering, Krishna Institute of Engineering and Technology, Meerut Road, Delhi-NCR, 201206 Gaziabad, Uttar Pradesh, India

ramsha004mtece19@igdtuw.ac.in, pragyasrivastava.19jun@gmail.com, richayadav@igdtuw.ac.in, richa.srivastava@kiet.edu

Abstract. *Leading digital circuits namely register, flipflops, state machines and counters drive operational aspects and potential applications in Integrated Circuit (IC) industry. MOS Current Mode Logic (MCML) based implementations with rapid response and simultaneous generation of complemented output is all set to become indispensable in nano regime industry. This paper attempts to optimize and address performance-based analysis of digital circuits namely NAND, D flipflop and 3-bit asynchronous counter by practicing MCML based implementation. These circuits are contemplated on four design parameters namely delay (t_p), power (pwr), Power Delay Product (PDP) and Energy Delay Product (EDP). This research focuses on relative analysis and emanate a salient optimal application of Complementary Metal-Oxide-Semiconductor (CMOS) and Carbon Nanotube Field Effect Transistor (CNFET) based 3-bit asynchronous counter. In addition to this, the two configurations of the MCML counter are then compared against applied V_{DD} at 16-nm technology nodes using HSPICE simulator. CNFET based 3-bit MCML counter is observed to be much faster (9.75×), significant improvement in gross power dissipation (11.93×), material refinement in PDP and EDP (116.39× and 1165×) respectively as compared to the conventional counterpart. Therefore, CNFET based implementations comes to the fore as resilient technology supporting high level integration in nano scale regime.*

Keywords

CMOS, CNFET, EDP, low power, MCML, PDP, propagation delay.

1. Introduction

The ascending urbanity of digital employment in the volatile industry is impelling the IC to advanced levels of intricacy. The steady fall in the chip size and corresponding rise in the chip density are emerging concern in terms of power consumption. Historically, bulk MOSFET's were appraised as the only feasible solution to convince the prominent Moore's law which afirmed that the count of transistors integrated on microchip will double about every two years. Moreover, the chip performance was synchronous with the overall circuit speed. There is also an immediate correspondence between the area on the chip and associated cost. As the implementation area increases it results in an increased packaging cost along with reduced fabrication yield. In 1999, researcher [1] proposed a New Complementary Metal-Oxide-Semiconductor (CMOS) exclusive OR (XOR) Circuit with Complementary XNOR function which resulted in full voltage swing and negligible static power. Although the transistor count reduced from 8 to 6, longer propagation delay due to the feedback structure was encountered as a major drawback.

Over the past three decades, researchers have been involved to design and simulate circuits with the help of state-of-the-art technology. One such technique entails an aspiring logic style in an analog friendly environment and subsides the power consumption of a compact structure popularly known as MOS current Mode logic [2]. Today power reduction is a primary concern in fields of circuit realization. The overall power consumption is a function of load capacitance and the supply voltage. Moreover, CMOS implementations techniques have gained consideration majorly because of its low power delivering expertise [3].

The current bias current source (I_{ss}) drawn in the MCML circuit is deduced from constant current bias source. The primary function of MCML relies on the current driven by the two circuit branches [4]. MCML has put forward a new di gained immense attention in the industry due to reduced process sensitivity along with minimal switching noise. This style has come up as speedy diferential style with outstanding power profile and large operating speed [5]. It stands as an excellent contender for static CMOS circuits [6]. Additionally, MCML technology exhibits enticing property of lower voltage swing along with exclusive diferential operation of the circuit. These circuits are barely prone to any switching noise and supply variations when compared with the CMOS counterpart logic style which tolerates significant noise. Eventually, MCML based circuits have immense application where high noise immunity and low supply noise generation is preferred. This succession permits the integration of digital and analog blocks onto the same chip [7]. Therefore, these apprising characteristics of MCML gives fruitful results in terms of power in a mixed signal environment and thus recognizes wide applications in the field of optical communication and ring oscillators [8].

However, the MCML logic style has inevitable imperfections that limit its usage to an extent. It has relatively high-power consumption at very low- frequencies, which makes it incompatible for its application in low-frequency applications. Moreover, MCML designs also requires steadfast fabrication technologies to perceive large load resistors. Implementing such resistors in turn increases the cost and the overall area of the integrated chip.

The first study of MCML in [9] considered Dynamic Current Mode Logic (DyCML) recognizing reduced swing logic style which was responsible for minimized gate and interconnect power dissipation. On comparing this design style with the most popular logic styles, DyCML circuits showed better delay, power-delay and energy-delay products. In 2002 [10] performed a research project proposing MCML Gate design and related optimization along with the MCML gate layout and studied the voltage swing of the circuits. Previous

work in [11] proposed novel GDI technique for low-power design. Up to 45 % reduction in overall PDP, significant improvement in the performance, as well as decreased transistor count were observed and thus proved as an advantage of GDI over CMOS and PTL. It is evident from the past discoveries [12] and [13] that the MCML logic style can successfully achieve favorable high-speed operation while dominating the power consumption at high frequencies.

The research article [14] presents frequency divider designed with the help of the MCML latch. Minimized power consumption is extracted by exploiting voltage gain, the ratio between the input period and the time constant and output swing, respectively, at single-ended output node and thus narrowed transistor sizing is also perceived. Researchers in [15] have realized XOR circuit with optimized design metrics. These include having lower PDP and reduced propagation delay. The authors in [16] have studied a Current Mode Logic (CML) based three-bit parity checker wherein switching the XOR gate inputs afects the size of the minimum test set. The authors in [17] have carried out an intense study to implement Robustness analysis to optimize the power dissipation of Load controller. Moreover, Layout of the proposed MCML adder has been proposed and designed. The authors in this paper [18] have proposed fast, low power, minimal noisy 1-bit full adder circuit that ofers lowered delay with increasing temperature and thus improved PDP. 32-bit ripple carry adder is implemented using the proposed design for ultra-low power applications. In [19], low voltage topology to implement MCML XOR gates is introduced and compared with 40 nm CMOS process. The proposed circuit works at minimum supply voltage by exploiting a threshold lowering technique and due to its capability to work with lower VSWING. The desire to operate a circuit at low supply voltage bearing minimum power consumption with reduced transistor count has led the authors in [20] to present novel Floating Gate MOSFET (FGMOS) based diferential voltage squarer using FGMOS characteristics in saturation region. The circuit provides a current output proportional to the square of the diference of two input voltages leading to optimized performance of the proposed circuit.

The innovations delegating numerous compact products are put through electronic elements with data storage capabilities. DFF also known as cyclic logic circuits are part of digital world that take this into account. They are able to store one bit of information and have pair of stable states namely 0 and 1. The outputs of these sequential circuits depends on both the past and present inputs [21].

Much work on the potential of D-FF has been carried out in the field of electronics over the years.

In [22], each transistor is sized warily while designing D-FF to get primary tradeof between propagation delay and power supply. Transistors are scaled to bring down the complete power consumption of the integrated circuit. In fact, according to [23], a highly compressed transistor is always at risk from random variations, which results in massive performance variations in D-FF.

A recent analysis discovers the concepts of metastability of D-FF and perceived high hold time and zero setup time consequently [24]. In [25], the literature brings our focus on the relative analysis between conventional D-FF and the CML based D-FF keeping the power profile and delay in light. Several researchers in the field of Very Large Scale Integration (VLSI) industry, for instance [26] are evolved in research related to dynamic CML to construct a power eficient D-FF. Additionally, the work reported in [27] is a major contribution and intuitive study on Carbon Nanotube Field Effect Transistor (CNFET), based MCML 3-bit parity checker circuit. Researchers in [28] carry out the analysis of several XOR gate based on CNFET topology along with the variability analysis. Low power XOR stands superior in terms of performance. The research article [29] introduces LP-XOR circuit which is found to ofer least variability of PWR and PDP. Design of a wide bandwidth current conveyor is introduced at 32 nm technology node. The same circuit is further is realized using the CNFET, which proves its robustness against PVT variation. Low power is dissipated as compared to CMOS counterpart. The researcher in this work [30] investigates variability analysis of the CMOS and the MCML based XOR circuit in terms of PDP wherein Narrower spread in PDP at all examined V_{DD} establishes the MCML circuit as adaptable against process and supply voltage variants.

The main motive behind working out the CNFET topology would be to enhance and optimize performance of digital logic circuits with reduced power consumption at low supply voltage.

The researchers in [27] proposed a novel CNFET based MCML 3-bit Parity checker and investigated 3-bit parity checker for four design metrics at 16 nm technology node for both MCML and conventional topology, which resulted in superior performance of the MCML based design in terms of design parameters. Furthermore, this design was proposed with the help of CNFET based implementation. The research article [31] proposed implement a novel design of 4-Bit 4-Tube CNFET based ALU at 16-nm Technology Node using two topologies namely CNFET and MCML based implementation in terms of Power dissipation (PWR) and Energy-Delay Product (EDP) variability. The researchers in [32] proposed performance evaluation of high-speed low-power MOS based MCML T FF based on four

design metrics using the MCML topology. The article [33] discusses the performance evaluation of low power design of delay element comparative analysis between MOSFET-based CMOS Delay Element (M-CMOS DE) and a MOSFET-based MCML Delay Element (M-MCML DE).

This paper is divided into 7 sections. The Sec. 1. gives a detailed review on the state-of-the-art MCML topologies, the gap and how CNFET would be beneficial. Section 2. analyses conventional CMOS based NAND circuit (C-MB NAND). This circuit is examined on various device parameters at 16 nm technology node and the corresponding results are tabulated and plotted. In Sec. 3. , CMOS based NAND CIRCUIT USING MCML topology (MB-MCML NAND) is derived and the simulation results are then mapped and compared with C-MB NAND circuit. Section 4. presents CMOS based D Flipflop circuit (MB-MCML DFF) using MCML NAND circuit derived previously. The upcoming Sec. 5. and Sec. 6. propose an application: 3-bit MCML asynchronous counter using CMOS technology (3-bit MCML CMOS COUNTER) and an emerging technology CNFET (3-bit MCML CNFET COUNTER). Further the two applications are compared and investigated on four design metrics including PWR, delay (t_p), Power Delay Product (PDP), EDP. The conclusions of the critique appear in Sec. 7. where CNFET based 3-bit MCML counter is observed to be much faster ($9.75\times$), it significantly improves the gross power dissipation ($11.93\times$), material refinement in PDP and EDP ($116.39\times$ and $1165\times$) respectively, compared to the conventional counterpart. This work presents extensive simulations using HSPICE for 16-nm PTM (developed by the Nanoscale Integration and Modeling (NIMO) Group at Arizona State University (ASU) [34].

2. Analysis Of C-MB NAND Circuit

Complementary metal oxide semiconductor often abbreviated as CMOS is a well-known technology in modern chip design industry and is widely used as ICs all over the world. It is dominant semiconductor technology with very low power dissipation, high density of integration and high switching speed. These advantages gratify the miniaturization of the MOSFETs and the upcoming realization of high-density IC with eternally increasing speed. With the scaling in IC technology, reliability of highly integrated circuit is a rising concern in the VLSI industry.

Equation (1) states the CMOS power dissipation in circuit designs.
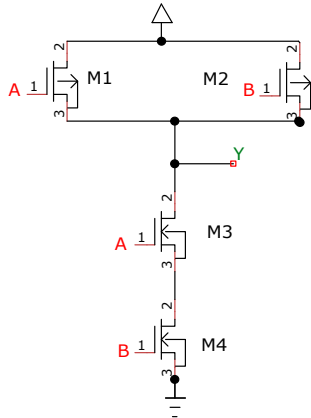
$$P_{total} = P_{static} + P_{dynamic}, \qquad (1)$$

Fig. 1: Schematic of C-MB NAND circuit.

wherein P_{total} is the total power, P_{static} is the static power and $P_{dynamic}$ is dynamic power.

Nowadays, delay and power are the two most noticeable metrics with a predominant tradeof in CMOS circuits. There is a need to improve these design metrics in order to extract enhanced operational speed and relative low power. This is thus given by the product of power and delay and is often known as PDP (see Eq. (2)).

$$PDP = pwr \cdot t_p, \qquad (2)$$

wherein pwr and t_p are the power dissipation and propagation delay of the circuit respectively.

But with the variation in input supply, the relative PDP falls significantly. To evade this efect, a prime parameter called as EDP comes into picture and is derived in the Eq. (3).

$$EDP = PDR \cdot t_p. \qquad (3)$$

Figure 1 shows the schematic diagram of C-MB NAND circuit. This circuit is then analyzed and investigated on four design metrics at supply voltage of 0.7 V and the corresponding simulation results are tabulated in Tab. 1. These simulated values are then plotted in Fig. 2.

Tab. 1: Design metrics of C-MB NAND circuit.

S.NO	Device parameters	C-MB NAND
1.	T_p (ns)	0.14
2.	PWR (PW)	34.49
3.	PDP (ZJ)	4.97
4.	EDP (ZJ-ns)	0.718

3. Analysis of MB-MCML NAND and its Comparison with C-MB-NAND Counterpart

3.1. MCML Design

As stated in the introduction, the MCML belongs to a logic family that deliver peculiar performance in terms of robustness, speed of operation and switching noise. Throughout the paper, the term MCML has been referred to MOS current mode logic.

The basic framework of the MCML logic circuit consists of Pull Up Network (PUN) at the source terminal, a Pull-Down Network (PDN) at the sink and a constant bias current source (I_{ss}).

As depicted in Fig. 3, The PUN is implemented using resistors (or PMOSs). And the PDN consists of distinct arrangement of NMOS transistors that accounts for realization of Boolean expression.

The eminent behavior of C-MB NAND circuit as discussed in the previous section gives an insight for recommended configuration of the CMOS circuit. This section discusses the implementation of MB-MCML NAND circuit and Fig. 4. shows the subsequent schematic diagram of MB-MCML NAND circuit.

MB-MCML NAND circuit is explored on four parameters including propagation delay, power dissipation, PDP and EDP at supply voltage of 0.7 V. The simulation analysis of the MB-MCML NAND circuit is depicted in Fig. 5.

Both NAND based implementations are imitated for 16 nm Technology node at 0.7 V supply (V_{DD}). HSPICE results of conventional circuit design and the proposed circuit design are set out in Tab. 2.

Tab. 2: Design metrics of MB-MCML NAND.

S.NO	Device parameters	C-MB NAND	MB-MCML-NAND
1.	T_p (ns)	0.14	0.009 (15.55)
2.	PWR (PW)	34.49	1.142 (30.20)
3.	PDP (ZJ)	4.97	0.011 (451.81)
4.	EDP (ZJ-ns)	0.718	0.0001 (7180)

From Tab. 2, it can be inferred that MB-MCML NAND circuit indicates 15.55× improvement in delay, 30.20× improvement in power, 451.81× improvement in PDP and 7180× improvement in EDP. The remarkable results of this circuit give out lower propagation delay and capitulate analog friendly environment when compared to counterpart. The MCML based design has shorter propagation delay due to its low voltage swing property than the latter. As an impact of de-
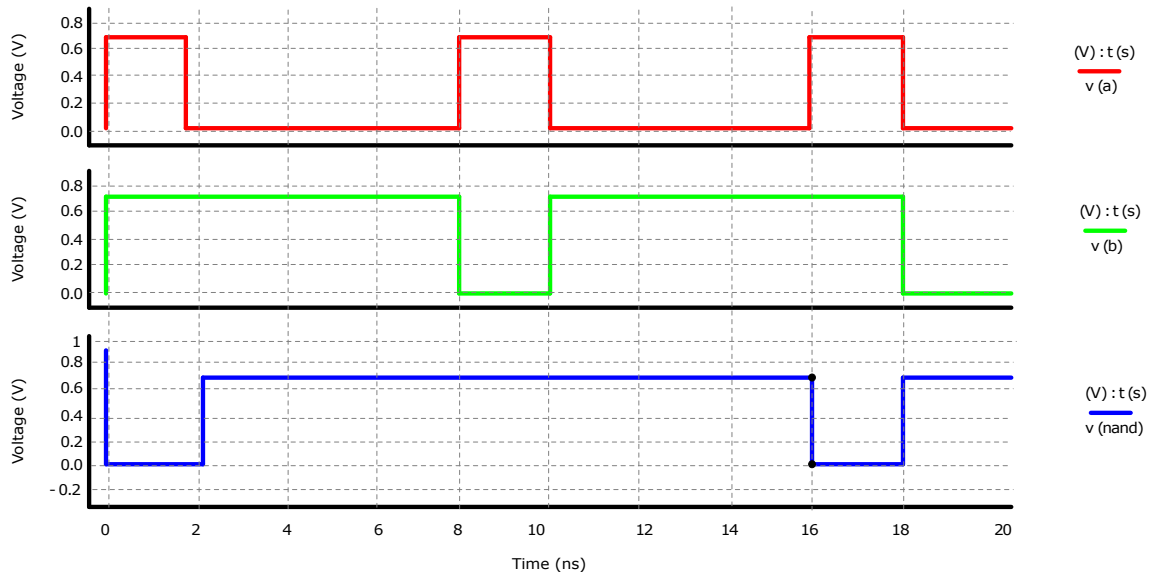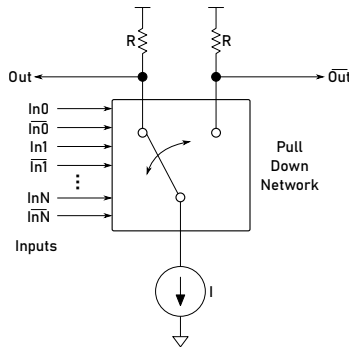
Fig. 2: Simulation results for C-MB NAND circuit.
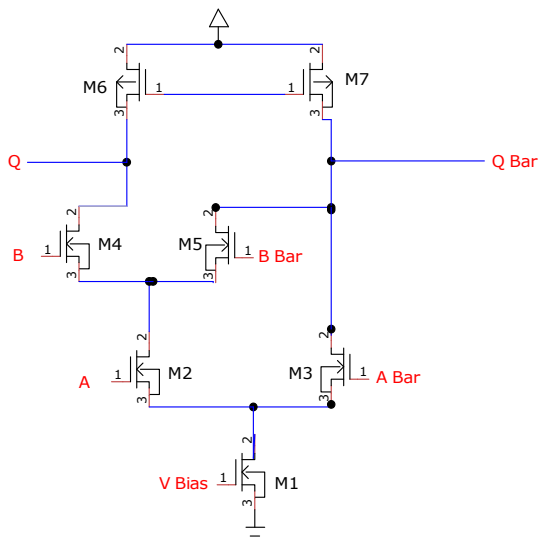

Fig. 3: Basic circuit of MCML gate [2].

Fig. 4: Schematic of MB-MCML NAND circuit.

lay, this PDP and EDP are also improved. As stated in Eq. (3) and EDP and PDP are directly related to delay, so when delay reduces, the corresponding EDP AND PDP also reduces.

Voltage swing also acts as an important factor of supply voltage. It defines a voltage range that impart an amplified and modified output without any deformation. The MCML is a reduced voltage swing logic. To reduce the overall propagation delay of a logic circuit, it is extremely desirable to obtain a reduced voltage swing.

According to the research done in [35], authors investigated the performance of static CMOS logic circuits and MOS Current Mode Logic (MCML) circuits in sub-threshold region. In order to operate the MCML circuit, the transistor constituting PDN was made to function by scaling down gate voltages. The control voltages were further scaled in order to retain the current source transistors in ohmic region while keeping the load transistors in linear region. The calculations for voltages and current are stated in Eq. (4) and Eq. (5) as follows:

$$V_{OH} = V_{DD} - R_1 \cdot I_{of}, \quad (4)$$

$$V_{OL} = V_{DD} - R_2 \cdot I_{on}, \quad (5)$$

where, V_{OH} is the maximum value of output voltages, V_{OL} is the minimum value of output voltages. R_1 is the resistance profered by a PMOS when $V_{DS} = V_{OH} - V_{DD}$ and R_2 is the resistance of a PMOS when $V_{DS} = V_{OL} - V_{DD}$. Also, I_{on} and I_{of} are the maximum and minimum current in the two branches of the diferential pair. On subtracting the two equations i.e. (Eq. (4) and Eq. (5)), we get:

$$V_{OH} - V_{OL} = (R_2 \cdot I_{on}) - (R1 \cdot I_{of}), \quad (6)$$

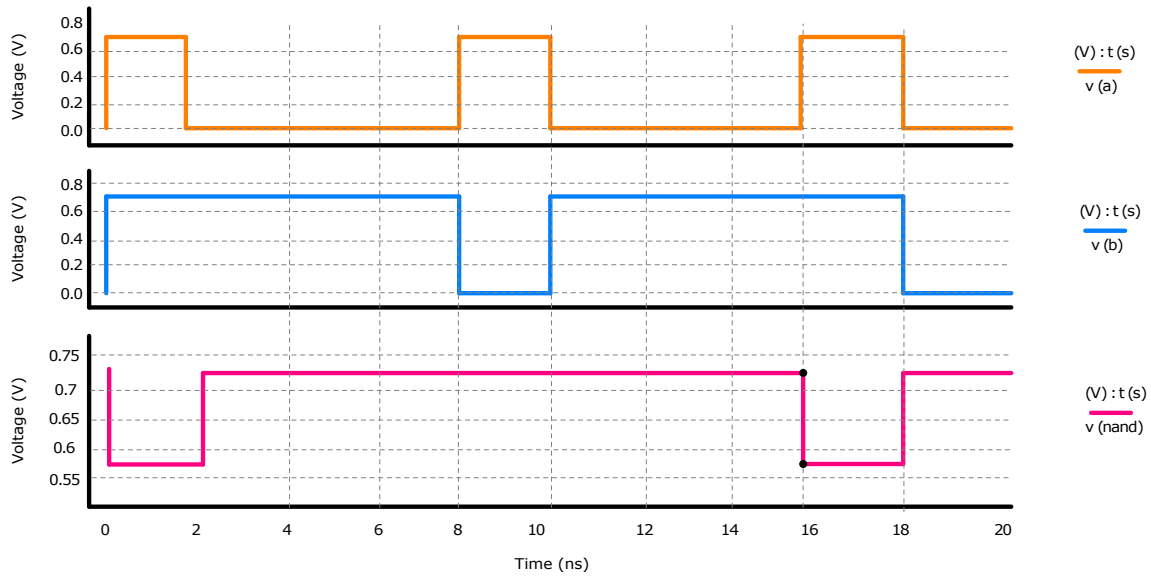$$\Delta V = R_2 \cdot (I_{on} - k \cdot I_{of}). \quad (7)$$

Fig. 5: Simulation results for MB-MCML NAND circuit.

The Eq. (7) shows how output voltage swing depends on the two currents wherein k is a constant.

The simulation graph in Fig. 2 shows the voltage swing of 0–0.7 V whereas the simulation graph depicted in Fig. 5 indicates swing of 0.55–0.7 V, thus implying significantly lowered voltage swing, making it applicable to high-speed operations. Therefore, these results have encouraged the author to utilize the MCML technique for reducing the overall power in the IC circuit at much higher frequencies. This paper also helps in validating the practicality of the MCML implementations. Further, this work ponders considerable insight on designing MB-MCML DFF circuit.

4. Implementation of MB-MCML-DFF Circuit

Among the various FF available, D-FF or Data / Delay FF is a fundamental FF that maps a circuit with digital sequential logic. It is an essential clock that latch, store and memorize the data. This edge triggered device transmit data input to one of the outputs on falling or rising edge of clock cycle. The symbol of this single input device and the corresponding circuit is constructed with the help of SR latch using NAND gates (as shown in Fig. 6 and Fig. 7). NAND gate being a universal gate can accomplish basic operations and perform many practical logic circuits due to the presence of transistors of same sizes.

The smooth performance of the MB-MCML NAND offers a brisk realization for scheming complex layout of the integrated logic circuits.
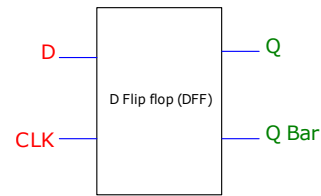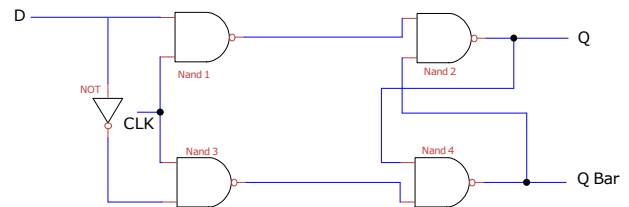

Fig. 6: Circuit symbol of D FF.

Fig. 7: D FF using NAND gate.

This section of the paper emphasizes on utilizing the above results to design MB-MCML DFF topology. The MB-MCML D FF is mapped using four NAND gates wherein each NAND gate is derived with the help of the MCML technique. The schema of the D-FF can be visualized in Fig. 8. Moreover, intriguing circuit employs 28 transistors and deliver output along with its compliment concurrently. Figure 7 is gate level diagram of DFF using NAND gate. Figure 8 is transistor level of MB-MCML-DFF. Figure 8 comprises of four subcircuits, each of this circuit represents a two input MCML NAND. Using the series gate approach, four MB-MCML NAND are connected together to configure MB-MCML D FF as manifested in Fig. 8. However, the schematic of two input MCML NAND is shown in Fig. 4.

This circuit is then explored and analyzed on four design facets specifically delay, power, PDP and EDP

Tab. 3: Design metrics of MB-MCML D FF and similar state of art.

S. No.	Design	Propagation delay	Power dissipation	PDP	EDP	No. of transistors
1	DESPFF [36]	4 ns	1990 µW	7.96 pJ	–	18
2	DESAFF [36]	2.5 ns	1420 µW	3.55 pJ	–	25
3	DENFF [36]	5.2 ns	347 µW	1.80 pJ	–	22
4	DEPFF [36]	7.3 ns	140 µW	1.022 pJ	–	20
5	MB-MCML-DFF (proposed)	0.04 ns	9.9 µW	0.47 aJ	0.02 aJ-ns	28

for the proposed MCML circuit. The HSPICE results of proposed circuit design of MB-MCML D FF are set out in Tab. 3.

Achieving a definite voltage swing between two significant levels of minimal threshold and noise immunity is liable for lessen delay of MCML technique in this work. Also, trivial power dissipation is achieved by proposed circuit design at submicron aspect (typically 16 nm) at V_{DD} -0.7 V for a bias current I_{bias} 10 µA and load capacitance of C_L 5 pF.

The work proclaimed till now has been proved and successfully published as evident in [37].
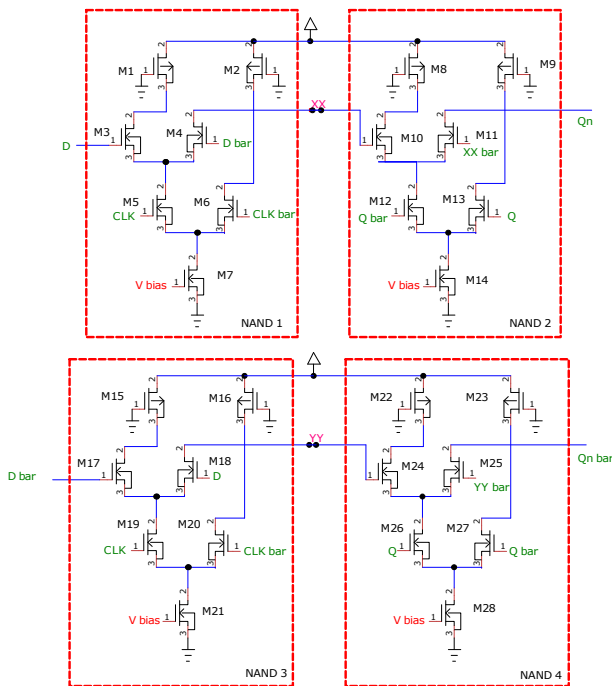

Fig. 8: Schematic of MB-MCML D FF.

5. Implementation Of MCML 3-Bit Asynchronous Counter Using CMOS Topology

As a continuation of the approach applied in MB-MCML D FF, this segment brings in a 3-bit asynchronous up counter. Since the aim

as mentioned in the introduction was to propose 3-bit up counter using CMOS technology, it has been performed by cascading three MB-MCML DFF as discussed in the previous section to acquire the desired circuit (Fig. 9). The clock feed of the three flip flops is cascaded and the Delay/ data input of all the flipflops is attached to the state output of the flipflop. This implies that each flip flop toggles at active edge of the clock feed. The first flip flop receives the clock input. The other two flip flops in the 3-bit counter acquire the clock input from the output Q bar of the preceding flipflop. On the occurrence of the active edge of the clock signal, the corresponding output of the first stage will toggle. All three D-FF in 3-bit asynchronous up counter are connected in the toggle mode. The rising edge of the main output Q of each stage encourages to trigger the clock signal to its succeeding flipflop. Eventually, the next clock frequency is triggered to half of the applied input.
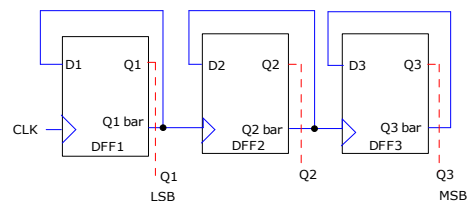

Fig. 9: Block diagram 3-bit MB-MCML COUNTER.

The transistor level configuration of a 3-bit MB-MCML COUNTER will constitute 84 transistors. The proposed circuit of 3-bit asynchronous counter using MB-MCML DFF as visualized in Fig. 7 was simulated on HSPICE simulator. Furthermore, the proposed application is determined for various design metrics to examine the overall speed and power probe and they are listed in the Tab. 4.

Tab. 4: Design metrics of 3-bit MB-MCML COUNTER.

S.NO	Device parameters	MB-MCML-COUNTER
1.	T_p (ns)	0.05
2.	PWR (µW)	29.84
3.	PDP (AJ)	1.492
4.	EDP (AJ-ns)	0.0746

6. Implementation of MCML Based 3-Bit Asynchronous Counter Using Carbon Nanotube Field Effect Transistor (CNFET) Topology

Fig. 10: Block diagram of 3-bit CNFET-MCML COUNTER.

The acronym CNFET denotes Carbon Nanotube Field Effect Transistor. In recent years there is growing interest in the field of CNFET technology as growth to silicon-CMOS due to tremendous characteristics of the circuit. The fundamental structure consists of carbon nanotubes placed horizontally wherein the nanotubes are composed of ultra-thin graphene sheets. These sheets are further rolled up in a form of void cylinders with preferable diameter between 0.4 mm to 4 mm [38] and [39]. The thin long Carbon Nanotubes (CNT) further attached to the transistor terminals (namely, source and drain) and has potential to establish a single path between them. CNFETS are believed to impart outstanding electrical properties for providing desirable strength to the device. An increasing number of studies have found that a digital circuit that employ n number of CNT's per CNFET commend n times faster response than any other CMOS topology [39] and [40].

The previous section successfully proposed implemented MCML 3-bit asynchronous counter using CMOS topology. The reduced voltage swing exhibited by MCML topology, assisted in realizing scaled power consumption, PDP and EDP, respectively.

Turning now to the second part of the proposal, the present section aims to implement and analyze 3-bit MCML asynchronous counter using CNFET (3-bit CNFET-MCML COUNTER). The working of CNFET DFF is similar to the working of MB-MCML D FF as explained in the previous section. Ballistic transport mechanism in CNFET based logic circuits enables faster response time and enhanced device parameters like PDP and EDP at low supply voltage making it more suitable for advanced applications. In line with the ballistic transfer of charging companies, their free-range approach is larger than the size of the device, which, in turn, facilitates fewer roadblocks between source and drain. Therefore, this is the impetus for improved transport carriers in CNFET rather than in CMOS-based circuits. Figure 10. represents a distinct block diagram of 3-bit MCML asynchronous counter trading CNFET technology.

In an attempt to work out eficient aggregates, the proposed circuit is computed at input supply of 0.7 V V_{DD} as per the ITRS guidelines, and is furt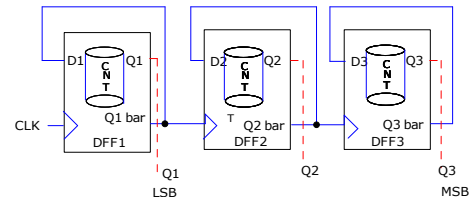her simulated on 16 nm technology node using HSPICE software. The proposed circuit schematic of 3-bit CNFET-MCML COUNTER is visualized in Fig. 11. Moreover, intriguing circuit employs 84 transistors and deliver output along with its compliment concurrently. Surprisingly no new transistors are required to extract the complimented result. The determined circuit is further evaluated for four design metrics specifically propagation, delay, power, PDP and EDP. The corresponding design parameters are further enlisted in the Tab. 5 as follows. Additionally, the analyzed results are then compared with the results drawn in Tab. 4 of the preceding section.

It is clear from Tab. 5 that the proposed application, CNFET based 3-bit MCML counter is faster (9.75 times), it provides significant improvement in gross power dissipation (11.93 times), material refinement in PDP and EDP (116.39 times and 1165 times respectively). The results shown in Tab. 5 can are presented in Fig. 12.

3-bit CNFET-MCML counter is proved to be faster than 3-bit MB-MCML counter due to ballistic transport mechanism. Moreover, 3-bit CNFET-MCML counter is found consume less power when compared to the counterpart 3-bit MB-MCML counter. Ballistic transport mechanism in CNFET thereby enables the integrated circuit to execute rapidly and consequently steer improved device metrics, PDP and EDP to name a few. In accordance to ballistic transmission of charge carriers, their mean free path is greater than the device dimension, which in turn, aid fewer collisions in the course between source and drain. Thus, this is the impetus for enhanced mobility of charge carriers in CNFET than in CMOS based circuits. Therefore, making it more appropriate for new-fangled applications.

7. Results and Discussion

Impulsive discoveries and scrutiny in the present-day integrated chips gain ground to optimize speed and power profile. In today's schema of miniaturized proportions, the two design facets establish the survival of any electronic circuitry. The ruthless demand for low power and high speed has intimated the research purpose to optimize the electronic circuits for the same.

Tab. 5: Design metrics of CNFET based 3-bit MB-MCML COUNTER.

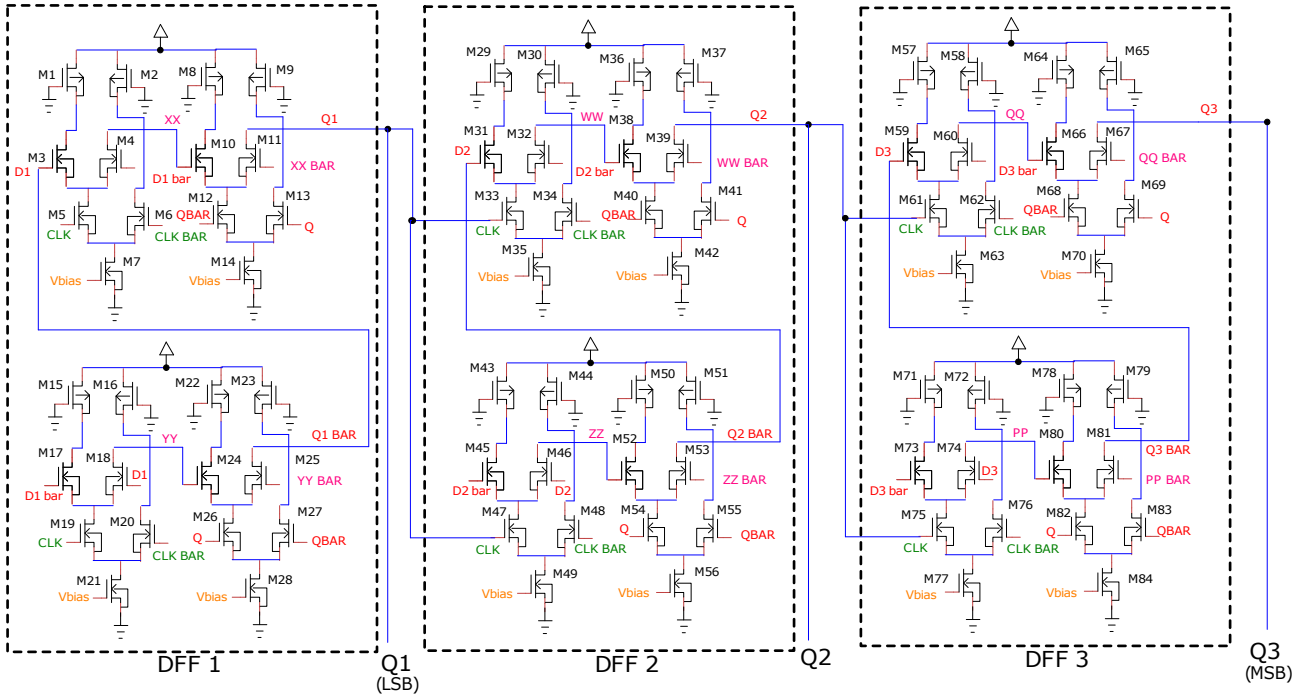| S.NO	Device parameters	MB-MCML-COUNTER	CNFET-MCML-COUNTER
1.	T_p (ns)	0.05	0.00512
2.	PWR (µW)	29.84	2.50125
3.	PDP (AJ)	1.492	0.01250
4.	EDP (AJ-ns)	0.0746	0.000064

Fig. 11: Schematic of 3-bit CNFET-MCML COUNTER.
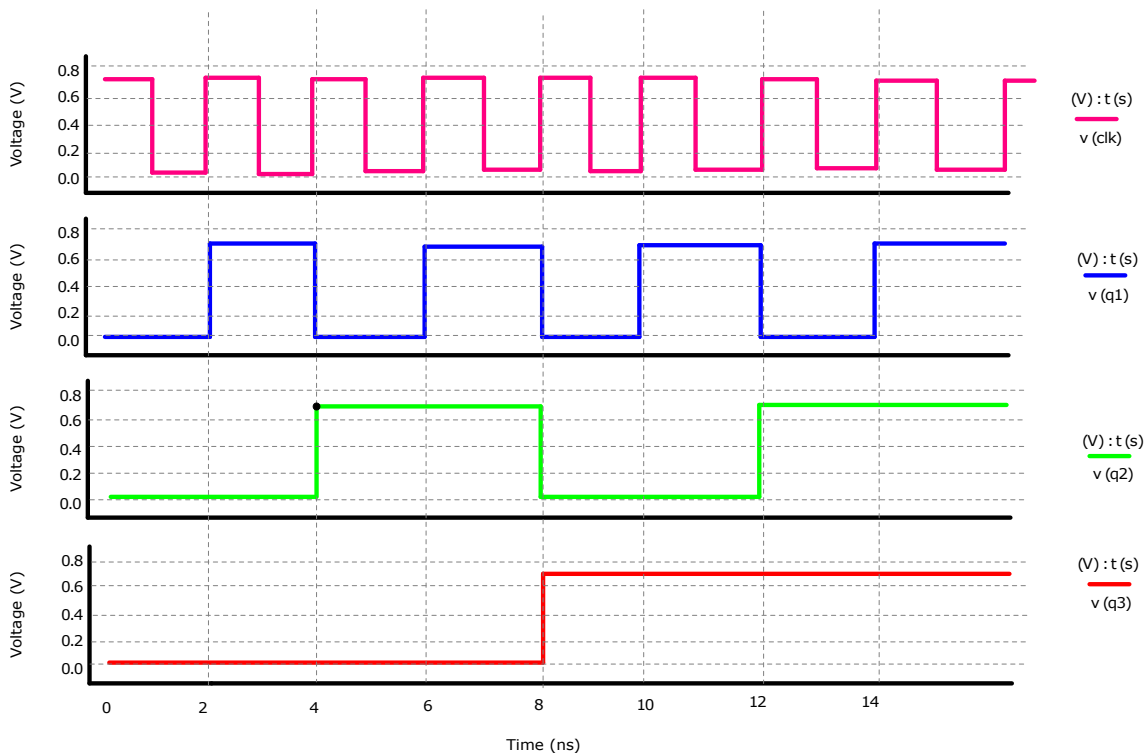

Fig. 12: Simulation results for 3-bit CNFET-MCML COUNTER circuit.

Copious applications and pertinent use of emerging technologies like CNFET in the recent electronics modules has motivated this work. This work investigated the conventional and MB-MCML NAND for propagation delay and speed and it can be inferred that MB-MCML NAND circuit indicates $15.55\times$ improvement in delay, $30.20\times$ improvement in power, $451.81\times$ improvement in PDP and $7180\times$ improvement in EDP, which is further validated by the simulation upshots of MB-MCML NAND. The remarkable results of this circuit give out lower propagation delay and capitulate analog friendly environment when compared to counterpart. Further this paper put forward a MB-MCML D-FF and soundly implements the integrated circuit at power supply of 0.7 V. Furthermore, 3-bit asynchronous MCML based counter is observed and examined at 16 nm technology taking CMOS and CNFET topologies into account. 3-bit CNFET-MCML COUNTER summed up to be a promising candidate thereby delivering phenomenal results. CNFET based 3-bit MCML counter is observed to be much faster $(9.75\times)$, it profers notable improvement in gross power dissipation $(11.93\times)$, material refinement in PDP and EDP $(116.39\times$ and $1165\times)$, respectively. compared to the conventional counterpart.The better performance of CNFET based 3-bit MCML counter can be explained for delay, power, EDP and PDP. The property of ballistic mechanism in CNFETs plays a vital role in enhancing the overall speed and hence the propagation delay of the circuit. Nowadays most of the digital designs have primary tradeofs between delay and power. These are, therefore, two design objectives that require balance in order to gain improved speed and related power and thus the product of the PDP enters the picture. However, in changing the input power supply, the PDP is significantly reduced due to the related delays decreasing significantly. To avoid this discrepancy, a low-power design parameter known as the EDP product is applicable. Taken together, these results underline the superiority of the MCML and CNFET technology as a solution to emerging concern in terms of power consumption in nano-regime industry performing MOSFET miniaturization. This paper gives a new horizon for ensuing research on low power profiles. All the circuit schematics were designed on Tiny-Cad 3.00.03.

Author Contributions

R.S. and P.S. developed the theoritical formulations, performed the analytic calculations along with the numerical simulations. Both P.S. and R.S. contributed to the final version of the manuscript. R.Y. and R.S. supervised the work. R.S. to the analysis of the results and R.S. drafted the final manuscript.

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About Authors

Ramsha SUHAIL is pursuing her Ph.D. from Indira Gandhi Delhi Technical University for Women (IGDTUW), New Delhi. She is currently working

in field of low power digital circuits.

Pragya SRIVASTAVA is pursuing her Ph.D. from Indira Gandhi Delhi Technical University for Women (IGDTUW), New Delhi. She is doing her research in the field of low power digital circuits.

Richa YADAV is working as an assistant professor in Indira Gandhi Delhi Technical University for Women (IGDTUW). She received her Ph.D. degree from the University of Delhi. Her research areas are low voltage low power digital circuit design, digital signal processing, designing of fractional order diferentiators and integrators, optimization of operators, evolutionary algorithms.

Richa SRIVASTAVA is working as an associate professor in KIET Group of Institutions, Ghaziabad. She received her Ph.D. degree from the University of Delhi. Her research focuses on design of analog and digital integrated circuits for low voltage/low power applications. She has thorough experience in working with various industry standard VLSI design tools (Tanner Electronics Design Automation (EDA); Cadence Virtuoso).