An Explicit Output Current-mode Quadrature Sinusoidal Oscillator and a Universal Filter Employing Only Grounded Passive Components - a Minimal Realisation

Tajinder Singh ARORA [1], *Manish GUPTA* [2], *Shiv Narain GUPTA* [3]

[1]Department of Electronics Engineering, National Institute of Technology, Uttarakhand, NH 58, 246174 Srinagar, India
[2]Department of Electronics and Communication Engineering, Inderprastha Engineering College, 63 Site IV, Sahibabad Industrial Area, Surya Nagar Flyover Road Sahibabad, 201010 Ghaziabad, India
[3]Department of Electronics and Communication Engineering, Jaypee Institute of Information Technology, A-10, Sector 62, 201309 Noida, India

tajarora@gmail.com, guptamanish2004@gmail.com, shivgnit@gmail.com

DOI: 10.15598/aeee.v19i3.4121

Article history: Received Feb 23, 2021; Revised Jul 06, 2021; Accepted Jul 07, 2021; Published Sep 30, 2021.

Abstract. *The use of voltage differencing current conveyor as an active device to design a current-mode oscillator along with a universal filter with only grounded passive elements is the main focus of this manuscript. This re-arranging circuit can work as a sinusoidal oscillator as well as a current-mode universal filter, by simple selection of passive switches. Both the circuits employ only two active devices and three grounded passive elements. The designed oscillator provides two distinctive current outputs with a quadrature-phase difference. It also maintains an independent condition of oscillation and frequency of oscillation. Moreover, the basic responses including low pass, high pass, and band pass are easily available from a current-mode universal filter. The low input impedance and high output impedance are amongst the noteworthy features of the current-mode derived filter. Non-ideal, parasitic, and sensitivity analysis of the designed circuits are also incorporated in the manuscript. Cadence PSPICE software simulation results are also included to justify the design idea. Experimental implementation of the described circuit has also been shown by employing special-purpose amplifier integrated circuit, i.e., OPA860.*

Keywords

Active filter, sinusoidal oscillator, Voltage Differencing Current Conveyor.

1. Introduction

The domain of analog signal processing is all about measurement, detection, and manipulation of the analog signals. Analog circuits find their applications in the area of control systems, communication engineering, instrumentation, and measurements [1]. Despite the dominance of digital signal processing, the analog signal processing finds its irreplaceable space in optical drives, analog to digital converters, etc. [2].

The rich culture of analog circuits is filled with multitudinous active devices. Few names in this long list are as follows: Current Conveyor (CC) [3] and [4], Operational Transconductance Amplifier (OTA) [5] and [6], Current Differencing Buffered Amplifier (CDBA) [7], Differential Voltage Current Conveyor (DVCC) [8], Current Differencing Transconductance Amplifier (CDTA) [9], Differential Voltage Current Conveyor Transconductance Amplifier (DVCCTA) [10], Unity Gain Cell (UGC) [11], Differential Difference Current Conveyor (DDCC) [12], Z-Copy Current Feedback Transconductance Amplifier (ZCCFTA) [13], etc. Each of the mentioned devices has its own uniqueness and features.

In [14], the authors proposed future looming devices, including Voltage Differencing Current Conveyor (VDCC). This is an electronic combination of OTA and

CC, and hence features/advantages of two different devices can be attained by this one device. The former input stage offers an electronically tunable transconductance (gm), whereas the latter stage conveys current from the input terminal to the output terminal. This active element is not explored and utilised up to its competence. The available applications in the open literature, realised with VDCC and its variants are mainly active filters and sinusoidal oscillators [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], and [27]. In a recent span of time, researchers have introduced different sinusoidal oscillators using different active building blocks. A comprehensive literature survey on the design of sinusoidal oscillators including VDCC has been performed; some prominent references which were taken into account are expressed in Tab. 1.

It can be summarised from Tab. 1 that:

- References [8], [9], [11], [28], [29], [30], [31], [32], [33], [34], [35], [36], and [37] do not utilise all grounded components.
- Higher number of passive elements are utilised in [8], [10], [11], [12], [15], [16], [17], [19], [28], [29], [30], [31], [32], [33], [34] [35], [37], [38], [39], [40], [41], and [42]; whereas higher count of active devices is encountered in [11], [13], [34], [41], [42], [43], [44], [45], and [46].
- Quadrature outputs are not available in [8], [10], [20], [28], [30], [33], [35], [40], and [43], whereas simultaneous availability of Current Mode (CM) and Voltage Mode (VM) is not provided by [9], [12], [13], [15], [16] [17], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [39], [40], [41], [43], [44], [45], and [46].
- Independent tunability of Condition of Oscillation (CO) along with the Frequency of Oscillation (FO) is not supported in references [8], [9], [16], [17], and [38].

There are only references [18], [19], [42], and [47] that fulfil all given constraints, but [19] and [42] use more passive elements, whereas [18] and [47] can work as an oscillator only (cannot perform the functions of an active filter). This manuscript is an attempt towards presenting a sinusoidal oscillator as well as a universal filter, both attained from the same configuration, employing VDCC and only grounded passive components. Designed circuits encounter the use of two passive switches, whose appropriate connection results in either an oscillator or a current mode active filter, delivering explicit current outputs in both cases. The fabrication of the circuit is also convenient as only grounded passive elements are used. The quadrature results are obtained in the oscillator circuit, in both CM as well as VM of operation. In the oscillator, CO and FO are independent and simple. The design of the universal filter provides all basic responses, like Low Pass (LP), High Pass (HP), Band Pass (BP), Band Reject (BR), and All Pass (AP).

The overall circuit offers low input and high output impedance, making it a preferable choice for cascading and for the realisation of higher-order filters.

The manuscript has been organized in various sections. The following section, i.e., Sec. 2. , will introduce the active device; VDCC. The designed configuration with its detailed ideal analysis is discussed in Sec. 3. Effect of non-idealities and sensitivity of design towards various elements is shown in Sec. 4. Section 5. details the effect of parasitic elements on the proposed circuit. The verification of the design through simulations has been represented in Sec. 6. and the justification of the same through experimentation is provided in Sec. 7. followed by concluding remarks.

2. Introduction to VDCC

The active device VDCC has in total six terminals namely P, N, Z, X, WP, and WN [22]. The input stage of the device has a current-controlled transconductance gain and a different current/voltage relationship between the different terminals, as given in Eq. (1).

$$\begin{bmatrix} I_P \\ I_N \\ I_Z \\ V_X \\ I_{WP} \\ I_{WN} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \\ I_X \end{bmatrix}. \quad (1)$$

The block diagram for the ideal VDCC is shown in Fig. 1. The realization of VDCC with Metal Oxide Semiconductor (MOS) transistors is shown in Fig. 2. The copy of the Z terminal named Zc− (for inverting output) and Zc+ (for non-inverting output) can also be found using MOS realization of the active device [19], as shown in Fig. 2.

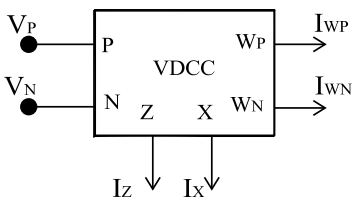

Fig. 1: Block Diagram of VDCC.

Applying the same concept [19], the copies of WP and WN terminals can also be realised, which have been named WPC and WNC, respectively.

Tab. 1: A comprehensive literature survey of sinusoidal oscillators including VDCC.

Ref. No.	Number of active devices employed	Number of used passive components	All grounded used passive elements	Availability of quadrature output	Attainment of independent CO and FO	Operating in both CM & VM
[8]	1	5	NO	NO	NO	YES
[9]	1	3	NO	YES	NO	NO
[10]	1	4	YES	NO	YES	YES
[11]	4	6	NO	YES	YES	YES
[12]	2	5	YES	YES	YES	NO
[13]	4	2	YES	YES	YES	NO
[15]	1	4	YES	YES	YES	NO
[16]	1	4	YES	YES	NO	NO
[17]	1	4	YES	YES	NO	NO
[18]	2	3	YES	YES	YES	YES
[19]	2	4	YES	YES	YES	YES
[20]	2	3	YES	NO	YES	YES
[23]	2	4	YES	YES	YES	NO
[24]	2	4	YES	YES	YES	NO
[25]	2	4	YES	YES	YES	YES
[26]	1	4	YES	YES	YES	NO
[27]	1	4	YES	NO	YES	NO
[28]	1	4	NO	NO	YES	NO
[29]	2	6	NO	YES	YES	NO
[30]	1	5	NO	NO	YES	NO
[31]	2	4	NO	YES	YES	NO
[32]	2	5	NO	YES	YES	NO
[33]	2	4	NO	NO	YES	NO
[34]	4	6	NO	YES	YES	NO
[35]	1	4	NO	NO	YES	NO
[36]	2	3	NO	YES	YES	NO
[37]	2	5	NO	YES	YES	NO
[38]	1	4	YES	YES	NO	YES
[39]	1	4	YES	YES	YES	NO
[40]	2	4	NO	NO	YES	NO
[41]	3	4	YES	YES	YES	NO
[42]	3	5	YES	YES	YES	YES
[43]	3	2	YES	NO	YES	NO
[44]	3	2	YES	YES	YES	NO
[45]	3	3	YES	YES	YES	NO
[46]	3	2	YES	YES	YES	NO
[47]	2	3	YES	YES	YES	YES
Proposed circuit	2	3	YES	YES	YES	YES

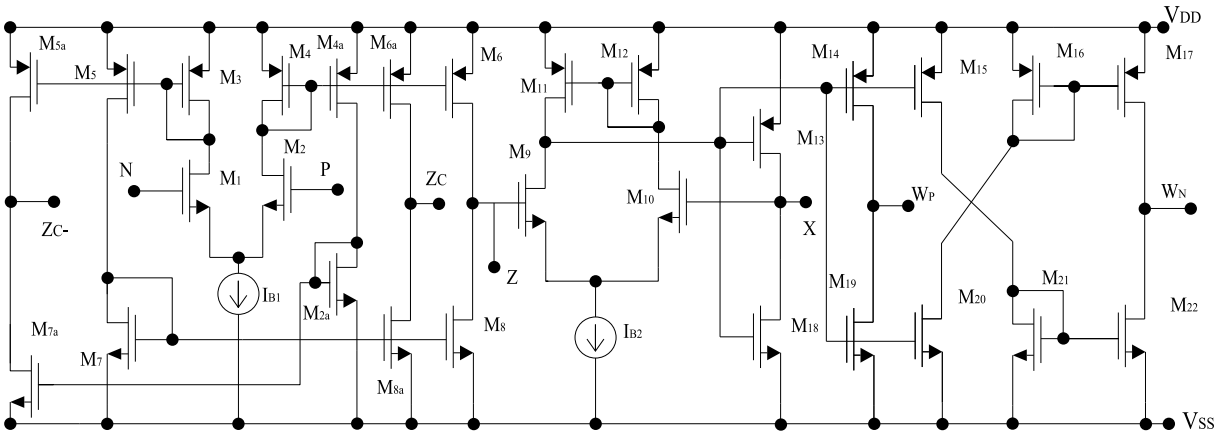

Fig. 2: CMOS realization of the Voltage Differencing Current Conveyor [19].

VDCC can also be implemented using commercially available Integrated Circuits (ICs), such as OPA 860 which is a special-function amplifier shown in Fig. 3. It is worth mentioning here that Fig. 3 is a modified version of figure of [21], which has been actively employed in this work.

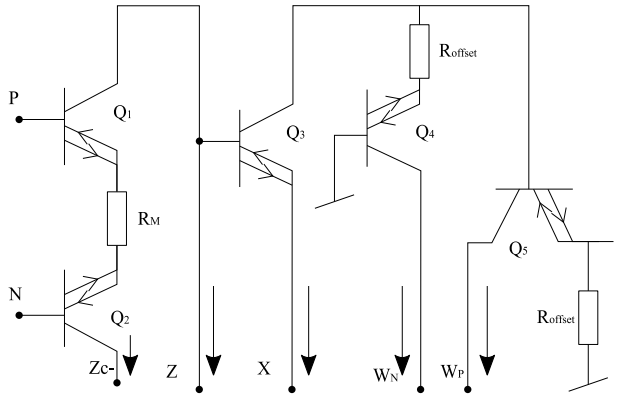

Fig. 3: Realization of VDCC utilizing discrete components.

3. Proposed Circuit

The proposed circuit diagram of a sinusoidal oscillator and a current mode active filter is shown in Fig. 4. This circuit can be converted from an oscillator to filter and vice-versa by appropriate selection of the passive switches i.e., S_1 and S_2, in Fig. 4. The patterns of engagement of these switches are given in Tab. 2.

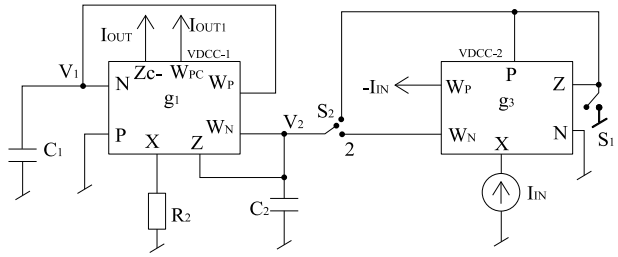

Fig. 4: Proposed circuit employing VDCC.

Tab. 2: Characteristic table for the proposed circuit.

S. No.	Switch position		Operation
	S_1	S_2	
1.	OFF	1	Dual-mode quadrature oscillator
2.	ON	2	Current-mode universal filter

Switch S_2 is the main switch that decides the functionality of the circuit, i.e., either filter or an oscillator. When switch S_2 is at position no. 1, the circuit works as an oscillator, otherwise, it acts as an active filter. The low input impedance for an active filter is achieved through switch S_1. When switch S_1 is in ON (closed) position, it makes Z terminal grounded offering low (zero) impedance at X terminal. Conversely, switch S_1 is kept in open (OFF) position for the oscillator application.

Appropriate connections of the switches (as shown in Tab. 2 at S. No. 1) result in a sinusoidal oscillator that can produce quadrature waveform in voltage mode as well as in the current mode. When simple fundamentals of circuit theory and techniques are applied to the designed circuit along with the characteristic equation of an ideal VDCC Eq. (1), we get the following equations given by Eq. (2), Eq. (3), Eq. (4), Eq. (5), and Eq. (6). The characteristic equation of the derived oscillator is represented in Eq. (2), whereas the CO and FO are represented in Eq. (3) and Eq. (4), respectively. Equation (3) shows that the CO can be independently tuned with the help of g_3 (transconductance factor of VDCC 2) without affecting the FO. It is worth noting here that FO can be electronically controlled from g_1 (the transconductance factor of VDCC 1) without altering the CO. The two output currents, i.e., I_{OUT} and I_{OUT_1}, are in quadrature with each other, as shown in Eq. (5). The relationship between the two voltages, i.e., V_1 and V_2, is shown in Eq. (6).

$$s^2 + \frac{s}{C_2}\left(\frac{1}{R_2} - g_3\right) + \frac{g_1}{R_2C_1C_2} = 0, \tag{2}$$

$$C \cdot O \cdot \left(\frac{1}{R_2} - g_3\right) = 0, \tag{3}$$

$$F \cdot O \cdot \omega_0 = \sqrt{\frac{g_1}{R_2C_1C_2}}, \tag{4}$$

$$\frac{I_{OUT}}{I_{OUT_1}} = \frac{g_1}{sC_1}, \tag{5}$$

$$\frac{V_1}{V_2} = \frac{g_2}{sC_1}. \tag{6}$$

When the switch combination of S. No. 2 from Tab. 2 is applied in Fig. 4, the proposed circuit works as a current-mode active filter. By simply applying the fundamentals of circuit simplification and the ideal equation of VDCC, i.e., Eq. (1), we get the following results for the current mode active filter. Eq. (7) and Eq. (8) show the responses of LP and BP filters. The rest of the responses, i.e., HP, BS, and AP, can be obtained as given in Eq. (9), Eq. (10) and Eq. (11). The common denominator polynomial along with angular frequency (ω_0) and quality factor (Q_0) are shown in Eq. (12), Eq. (13) and Eq. (14), respectively. Eq. (7), Eq. (8), Eq. (9), Eq. (10), and Eq. (11) justify the design idea of a universal filter.

$$\frac{I_{OUT}}{I_{IN}} = \frac{I_{LP}}{I_{IN}} = \frac{\frac{g_1}{R_2C_1C_2}}{D(s)}, \tag{7}$$

$$\frac{I_{OUT_1}}{I_{IN}} = \frac{I_{BP}}{I_{IN}} = \frac{\frac{s}{R_2C_2}}{D(s)}, \tag{8}$$

$$\frac{I_{HP}}{I_{IN}} = \frac{-I_{IN} + I_{OUT} + I_{OUT_1}}{I_{IN}} = -\frac{s^2}{D(s)}, \tag{9}$$

$$\frac{I_{BS}}{I_{IN}} = \frac{-I_{IN} + I_{OUT_1}}{I_{IN}} = -\frac{\left(s^2 + \frac{g_1}{R_2C_1C_2}\right)}{D(s)}, \tag{10}$$

$$\frac{I_{AP}}{I_{IN}} = \frac{I_{BS} + I_{BP}}{I_{IN}} = -\left(\frac{s^2 + \frac{s}{R_2C_2} + \frac{g_1}{R_2C_1C_2}}{D(s)}\right), \tag{11}$$

$$D(s) = s^2 + \frac{s}{R_2C_2} + \frac{g_1}{R_2C_1C_2}, \tag{12}$$

$$\omega_0 = \sqrt{\frac{g_1}{R_2C_1C_2}}, \tag{13}$$

$$Q_0 = \sqrt{\frac{R_2C_2g_1}{C_1}}. \tag{14}$$

4. Non-ideal and Sensitivity Analysis

In the preceding sections, we have considered only the ideal behavior model of the mentioned active device but this section of the manuscript deals with the non-ideal performance of VDCC. The characteristic equation while considering the non-idealities or commonly known tracking error of the device is given in Eq. (15) where α, β, γ_P, and γ_N are the tracking errors of the ports. Here, α is basically a transconductance error, β is the voltage transfer error between Z and X port and γ_P and γ_N are the tracking errors of W_P and W_N ports with respect to X terminal of the device.

When these non-ideal port transfer ratios/tracking errors are considered for interpreting the sinusoidal oscillator circuit (as given in Fig. 4), the following equations are derived. The characteristic equation is given by Eq. (16). The newly modified CO and FO are depicted in Eq. (17) and Eq. (18), respectively.

$$\left.\begin{array}{c} I_Z = \alpha \cdot g_m(V_P - V_N) \\ V_Z = \beta \cdot V_X \\ I_{WP} = \gamma_P \cdot I_X \\ I_{WN} = -\gamma_N \cdot I_X \end{array}\right\}, \tag{15}$$

$$s^2 + \frac{s}{C_2}\left(\frac{\beta_1\gamma_{N_1}}{R_2} - \alpha_2 \cdot g_3\right) + \frac{\alpha_1\beta_1\gamma_{P_1} \cdot g_1}{R_2C_1C_2} = 0, \tag{16}$$

$$C \cdot O \cdot \left(\frac{\beta_1\gamma_{N_1}}{R_2} - \alpha_2 \cdot g_3\right) = 0, \tag{17}$$

$$F \cdot O \cdot \omega_0' = \sqrt{\frac{\alpha_1\beta_1\gamma_{P_1} \cdot g_1}{R_2C_1C_2}}, \tag{18}$$

where α_1, β_1, γ_{P_1}, and γ_{N_1} are the non-ideal port transfer ratios of VDCC 1 and α_2, β_2, γ_{P_2}, and γ_{N_2} are the non-ideal port transfer ratios of VDCC 2. By considering the non-ideal behaviour of VDCC, the circuit of the active filter (as given in Fig. 4) is also interpreted. The obtained transfer functions for the LP and BP filters are shown in Eq. (19) and Eq. (20). The non-ideal angular frequency (ω_0') and non-ideal quality factor (Q_0') along with common denominator polynomial are represented by Eq. (21), Eq. (22), and Eq. (23), respectively.

$$\frac{I_{OUT}}{I_{IN}} = \frac{I_{LP}}{I_{IN}} = \frac{\alpha_1\beta_1\gamma_{P_1}\gamma_{N_2} \cdot \left(\frac{g_1}{R_2C_1C_2}\right)}{D'(s)}, \tag{19}$$

$$\frac{I_{OUT_1}}{I_{IN}} = \frac{I_{BP}}{I_{IN}} = \frac{\beta_1\gamma_{P_1}\gamma_{N_2} \cdot \left(\frac{s}{R_2C_2}\right)}{D(s)}, \tag{20}$$

$$\omega_0' = \sqrt{\frac{\alpha_1\beta_1\gamma_{P_1} \cdot g_1}{R_2C_1C_2}} = \omega_0\sqrt{\alpha_1\beta_1\gamma_{P_1}}, \tag{21}$$

$$Q_0' = \frac{1}{\gamma_{N_1}}\sqrt{\frac{\alpha_1\gamma_{P_1}R_2C_2 \cdot g_1}{\beta_1C_1}} = Q_0\left(\frac{1}{\gamma_{N_1}}\sqrt{\frac{\alpha_1\gamma_{P_1}}{\beta_1}}\right), \tag{22}$$

$$D'(s) = s^2 + s\left(\frac{1}{C_2}\right)\left(\frac{\beta_1\gamma_{N_1}}{R_2}\right) + \frac{\alpha_1\beta_1\gamma_{P_1} \cdot g_1}{R_2C_1C_2}. \tag{23}$$

The above-mentioned equations show that the ideal and non-ideal outputs (equations) are relatable, thereby justifying the designed idea. The sensitivity of both active and passive elements is considered for theoretical analysis. Here, the sensitivity analysis for ideal angular frequency (ω_0), non-ideal pole frequency (ω_0'), and quality factor (Q_0) and (Q_0' are scrutinised. Eq. (24) and Eq. (25) represent sensitivity calculation for ideal angular frequency (ω_0) and ideal quality factor (Q_0), whereas Eq. (26), Eq. (27), Eq. (28), and Eq. (29) represent non-ideal angular frequency (ω_0') and non-ideal quality factor (Q_0'). All these equations derived below show that the sensitivity in all the cases is under considerable limits.

$$S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = S_{R_2}^{\omega_0} = -\frac{1}{2}; \quad S_{g_1}^{\omega_0} = \frac{1}{2}, \tag{24}$$

$$S_{R_2}^{Q_0} = S_{C_2}^{Q_0} = S_{g_1}^{Q_0} = \frac{1}{2}; \quad S_{C_1}^{Q_0} = -\frac{1}{2}, \tag{25}$$

$$S_{\alpha_1}^{\omega_0'} = S_{\beta_1}^{\omega_0'} = S_{\gamma_{P_1}}^{\omega_0'} = \frac{1}{2}, \tag{26}$$

$$S_{g_1}^{\omega_0'} = \frac{1}{2}; \quad S_{C_1}^{\omega_0'} = S_{C_2}^{\omega_0'} = S_{R_2}^{\omega_0'} = -\frac{1}{2}, \tag{27}$$

$$S_{C_2}^{Q_0'} = S_{R_2}^{Q_0'} = S_{g_1}^{Q_0'} = \frac{1}{2}; \quad S_{C_1}^{Q_0'} = -\frac{1}{2}, \tag{28}$$

$$S_{\alpha_1}^{Q_0'} = S_{\gamma_{P_1}}^{Q_0'} = \frac{1}{2}; \quad S_{\beta_1}^{Q_0'} = -\frac{1}{2}; \quad S_{\gamma_{N_1}}^{Q_0'} = -1. \tag{29}$$

The recognised parasitic model of VDCC [18] has been taken into consideration to contemplate the effects on the proposed circuits. When the VDCC model of Fig. 5 is reintegrated into the proposed circuit of Fig. 4 (only when Fig. 4 is acting as a sinusoidal oscillator), the resultant configuration resembles, as shown in Fig. 6. Some assumptions and simplifications have also been made before evaluating the circuit and are presented in Eq. (30). The characteristic polynomial is represented in Eq. (31). The CO and FO including

device parasitics of the oscillator are shown in Eq. (32) and Eq. (33), respectively.

$$\left.\begin{array}{c} R_A = R_{P_1} \\ R_B = R_{Z_1}||R_{Z_2}||R_{N_1} \\ R_A >> R_{X_1} \\ C_A = C_1 + C_{P_1} \\ C_B = C_2 + C_{N_1} \end{array}\right\}, \tag{30}$$

$$\begin{aligned} &s^2 + s\Big(\frac{1}{C_A R_A} + \frac{1}{C_B R_B} - \frac{g_3}{C_B} + \frac{1}{C_B R_2}\Big) + \\ &+\frac{1}{C_A C_B}\Big[\frac{1}{R_A}\Big(\frac{1}{R_B} + \frac{1}{R_2} - g_3\Big) + \frac{g_1}{R_2}\Big] = 0, \end{aligned} \tag{31}$$

$$CO: \Big(\frac{1}{C_A R_A} + \frac{1}{C_B R_B} - \frac{g_3}{C_B} + \frac{1}{C_B R_2}\Big) = 0, \tag{32}$$

$$FO: \tilde{\omega}_0 = \sqrt{\frac{1}{C_A C_B}\Big[\frac{1}{R_A}\Big(\frac{1}{R_B} + \frac{1}{R_2} - g_3\Big) + \frac{g_1}{R_2}\Big]}. \tag{33}$$

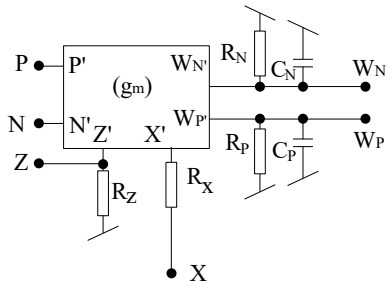

Fig. 5: Block diagram of VDCC including device parasitics [18].

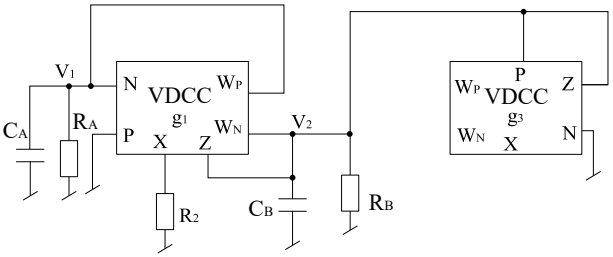

Fig. 6: Block diagram of electronically controlled oscillator including device.

When the derived circuit of a current-mode active filter (only when Fig. 4 is used as a universal filter) is reconfigured by replacing the ideal model of VDCC with the parasitic model of VDCC (from Fig. 5), the resultant structure looks as depicted in Fig. 7.

Before applying the regular circuit theory fundamentals to the derived circuit (Fig. 7), we have taken the following simplifications and assumptions, represented by Eq. (34), to conclude the outcome equations in a more suitable manner. The responses of LP and BP, including the effects of parasitic, are given in Eq. (35) and Eq. (36), respectively.

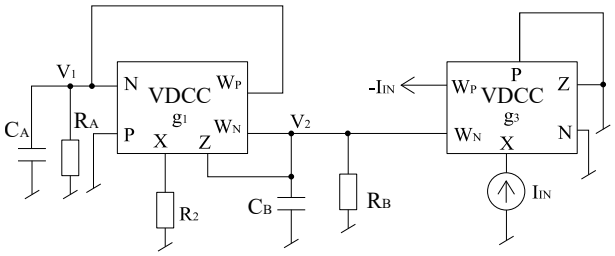

Fig. 7: Universal filter with device parasitics.

$$\left.\begin{array}{c} R_A = R_{P_1} \\ R_B = R_{Z_1}||R_{N_1}||R_{N_2} \\ R_2 >> R_{X_1} \\ C_A = C_1||C_{P_1} \\ C_B = C_2||C_{N_1}||C_{N_2} \end{array}\right\}, \tag{34}$$

$$\frac{I_{OUT}}{I_{IN}} = \frac{\frac{g_1}{R_2 C_A C_B}}{\tilde{\tilde{D}}(s)}, \tag{35}$$

$$\frac{I_{OUT_1}}{I_{IN}} = \frac{\Big[\frac{1}{R_A C_A} + s\Big] \cdot \frac{1}{R_2 C_B}}{\tilde{\tilde{D}}(s)}. \tag{36}$$

The denominator polynomial ($\tilde{\tilde{D}}(s)$), angular frequency ($\tilde{\tilde{\omega}}_0$), and quality factors ($\tilde{\tilde{Q}}_0$) are represented as Eq. (37), Eq. (38) and Eq. (39), respectively. It may be concluded from the above-given equations that both the derived circuits work well under the influence of the device parasitics.

$$\begin{aligned} \tilde{\tilde{D}}(s) = &s^2 + s\Big(\frac{1}{C_A R_A} + \frac{1}{C_B R_2} + \frac{1}{C_B R_B}\Big) + \\ &+\frac{1}{C_A C_B}\Big[\frac{g_1}{R_2} + \frac{1}{R_A R_2} + \frac{1}{R_A R_B}\Big], \end{aligned} \tag{37}$$

$$\tilde{\tilde{\omega}}_0 = \sqrt{\frac{1}{C_A C_B}\Big[\frac{g_1}{R_2} + \frac{1}{R_A R_2} + \frac{1}{R_A R_B}\Big]}, \tag{38}$$

$$\begin{aligned} \tilde{\tilde{Q}}_0 = &\frac{R_2 R_A R_B}{C_B R_2 R_B + C_A R_A R_B + C_A R_A R_2} \cdot \\ &\cdot\sqrt{C_A C_B\Big[\frac{g_1}{R_2} + \frac{1}{R_A R_2} + \frac{1}{R_A R_B}\Big]}. \end{aligned} \tag{39}$$

It may be concluded from the above-given equations that both the derived circuits work well under the influence of the device parasitics.

5. Simulation Results

The designed circuits have been tested to verify the theoretical results using Cadence PSPICE simulation software. Figure 2 has been used for representing the VDCC block, made up of MOS transistors. In Fig. 2, the bias supply requirements are

±0.9 V voltage source for voltage biasing and the values of I_{B_1} and I_{B_2} are 50 µA and 100 µA respectively, to get the value of transconductance factor (g_m) as 277 µA·V^{-1}. The simulation results are bifurcated as mentioned. Firstly, the simulations of an electronically controllable sinusoidal oscillator are shown, where the results achieved through simulations for the active filter are represented later. Aspect ratios used for Fig. 2 are taken from [18] shown in Tab. 3. Here, 0.18 µm CMOS process parameters used for simulations are taken from [48].

Tab. 3: Aspect ratios of the MOS devices.

CMOS Transistors	W·L^{-1} (µm)
M_1–M_4	3.6/1.8
M_5–M_6, M_{4a}, M_{5a}, M_{6a}	7.2/1.8
M_7–M_8, M_{2a}, M_{7a}, M_{8a}	2.4/1.8
M_9–M_{10}	3.06/0.72
M_{11}–M_{12}	9/0.72
M_{13}–M_{16}	14.4/0.72
M_{17}	13.85/0.72
M_{18}–M_{22}	0.72/0.72

For the simulations of the designed quadrature oscillator, the passive components are selected as $C_1 = C_2 = 43$ pF, $R_2 = 3.60$ kΩ. The transconductance factors are $g_1 = g_3 = 277$ µA·V^{-1}. To show the working waveform of the designed oscillator, Fig. 8 has been presented. The Fast Fourier Transform (FFT) of the same waveform is shown in Fig. 9.

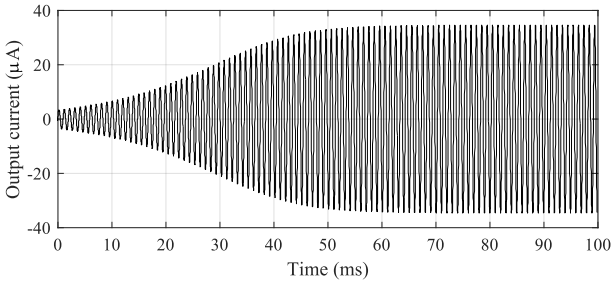

Fig. 8: Transient response for current-mode sinusoidal oscillator (I_{OUT}).

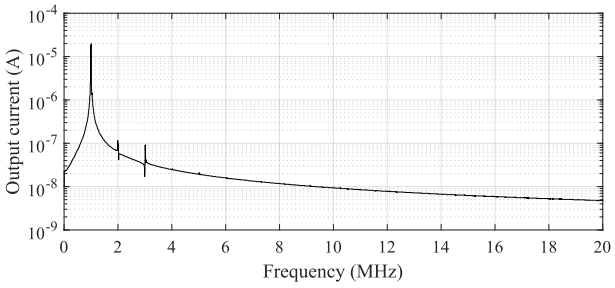

Fig. 9: Fast Fourier Transform of the I_{OUT}.

The theoretical value of the frequency of oscillation is chosen as 1.03 MHz. The simulated value of the frequency is achieved as 1.01 MHz, giving an error of 1.76 %. The deviation of oscillation frequency due to the effect of parasitics have also been calculated. The values of the parasitic elements have been taken from [19]. It is found that for the ideal frequency of 1.03 MHz, the computed oscillation frequency, under the impact of parasitics, is 1.0 MHz and gives an error of 2.72 %. The two distinct and explicit outputs, i.e., I_{OUT} and I_{OUT_1}, which must be theoretically phase-shifted by 90°, have been shown in Fig. 10. The calculated phase difference between the two signals in current mode is derived as 89.3°. The designed oscillator also provides voltage-mode quadrature outputs (the waveform of a few cycles only), as shown in Fig. 11.

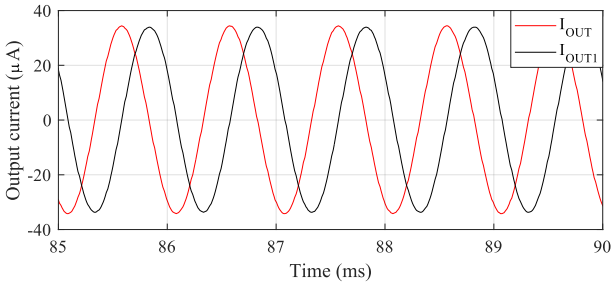

Fig. 10: Current-mode quadrature outputs.

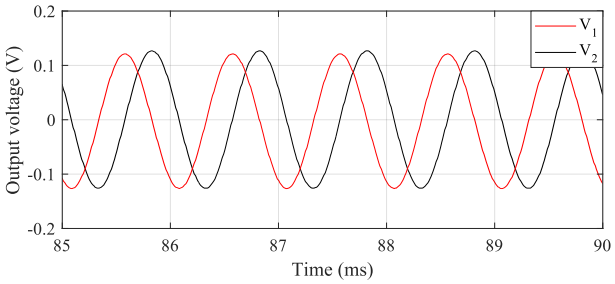

Fig. 11: Voltage-mode quadrature outputs.

The calculated angle difference between these two voltage signals is 89.2°. It can be seen from Eq. (4) that FO is directly dependent upon transconductance factor g_1. The same can be adjusted with the help of bias current, i.e., I_{B_1}, in Fig. 2 of the VDCC block. Thus, to check the wide span of the frequency of the oscillator, FO is varied with respect to the bias current of VDCC.

In Fig. 12, the value of I_{B_1} varies from 30 µA to 65 µA and the corresponding frequency ranges from 913 kHz to 1.08 MHz. If the bias current is further increased beyond this range, the active device gets saturated, increasing the percentage of error. The ideal and simulated values in Fig. 12 are closely related, thereby justifying the designed idea.

Theoretically, the designed circuit should deliver the constant output over the proposed range of frequencies. Unfortunately, while testing, the obtained responses did not match up with expectations. Variations in current outputs are shown in Fig. 13. Figure 14 shows the deviations in voltage mode quadrature outputs. It is evident from Fig. 13 and Fig. 14, that to get

stabilised output (s), either buffers or Automatic Gain Control (AGC) circuitry need to be deployed [49], [50], [51], and [52].

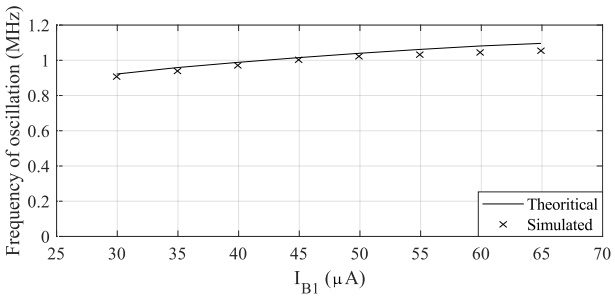

Fig. 12: Variation of frequency of operation with respect to bias current (I_{B_1}).

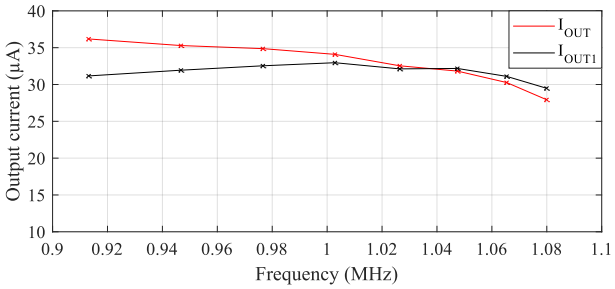

Fig. 13: Variation of current magnitude for sinusoidal oscillator.

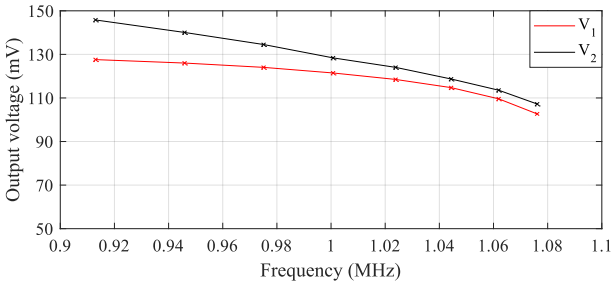

Fig. 14: Voltage variations with respect to oscillation frequency.

An already discussed approach for the utilization of AGC network [51] has been deployed in the designed oscillator. The output waveform at three different frequencies with almost the same magnitude is shown in Fig. 15, thus justifying the use of AGC network in the proposed oscillator.

Due to the brevity of the manuscript, the details of the AGC circuits are not discussed here and readers are encouraged to refer to the suggested references [49], [50], [51], and [52]. From Fig. 16, the phase dependency of the designed quadrature oscillator over a wide range of the frequency can be seen. To attain the constant phase difference between the two waveforms of quadrature oscillator, AGC circuit may be utilised. A graphical representation of oscillation frequency and corresponding Total Harmonic Distortion (THD) is represented in Fig. 17.

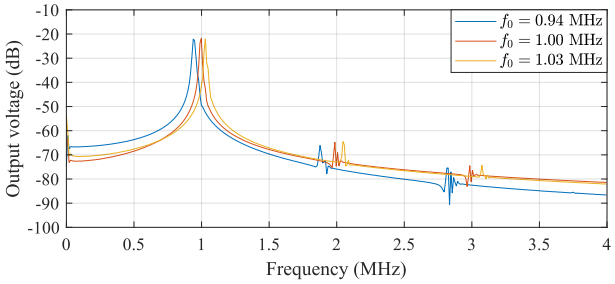

Fig. 15: Voltage variations with respect to oscillation frequency including AGC network.

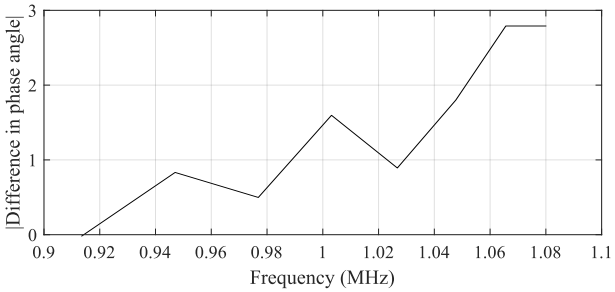

Fig. 16: Phase swing of a quadrature oscillator (current mode).

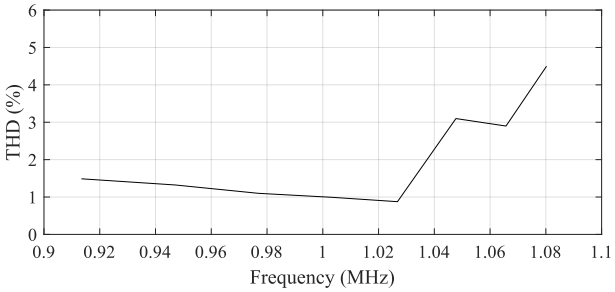

Fig. 17: THD values with respect to oscillation frequency.

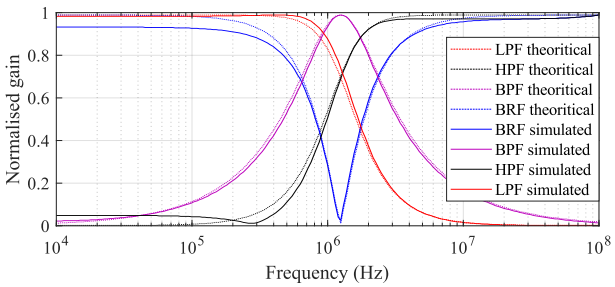

Fig. 18: Current-mode universal filter (LP, HP, BP and BR) responses.

To get the simulation results for a current-mode active filter, the values of the passive elements are $C_1 = C_2 = 50$ pF, $R_2 = 1.8$ kΩ, and $g_1 = g_3 = 277$ μA·V^{-1}. Figure 18 shows the ideal and practical frequency responses of LP, HP, BP, and BS filters. The calculated center frequency of the universal filter is 1.25 MHz,

whereas through simulation, 1.245 MHz was achieved giving an error of 0.4 % and therefore, supporting the design circuit. The following figure, i.e., Fig. 19, shows the gain as well as phase response of the AP filter. To see the fidelity of the filter circuit, transient analysis is performed on band pass filter. The response of the same is shown in Fig. 20. The frequency of the input sinusoidal signal is 1.25 MHz and the magnitude of the current is 50 μA. Figure 20 shows that the output is closely followed by the input.

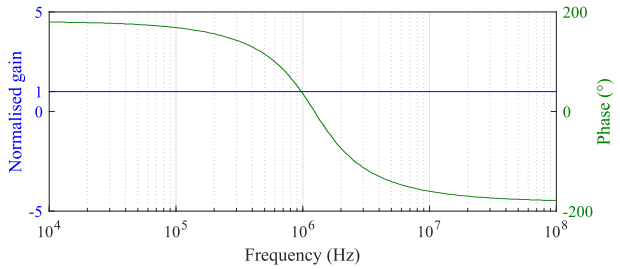

Fig. 19: All pass filter's gain and phase response.

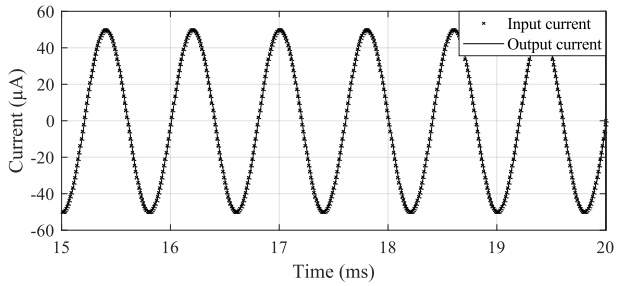

Fig. 20: Transient response of a BP filter.

The calculations for the THD of a BP filter have also been done, and its graphical representation is presented in Fig. 21. It is evident from Fig. 21 that the THD range of a BP filter is significantly low until the input magnitude of the current reaches a value of 120 μA.

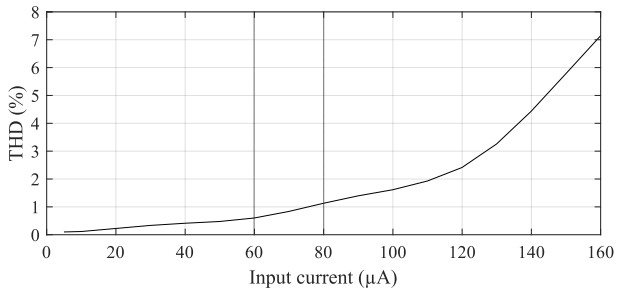

Fig. 21: A graphical representation of THD of a BP filter.

As discussed earlier, analogue circuits can find their applications in the area of control systems, communication engineering, instrumentation, and measurements [1]. In communication, Amplitude Modulation (AM) is one of the basic modulation techniques where the derived oscillator and designed filter circuit can occupy its space. The block diagram along with the waveforms' produced from the respective blocks have been shown in Fig. 22.

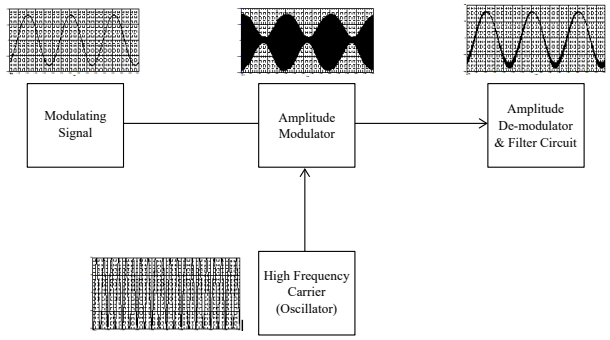

Fig. 22: Block diagram of Amplitude Modulation and Demodulation.

6. Experimental Results

There is no single commercially available Integrated Circuit (IC) that can successfully substitute the VDCC. Therefore, this active device is usually formulated from the combination of different off-the-shelf ICs. There are many approaches to realise this active building block such as (i) using LM13700 and AD844 [53], (ii) employing OPA860, (iii) using CA3080 and AD844. OPA860 is commonly known as the diamond transistor or special-purpose amplifier [54]. The approach utilised here is with the help of OPA860 due to the sterling features of this amplifier IC [54]:

- It is a special-function amplifier whose transconductance gain can be controlled with the help of single external resistor.
- The results obtained through OPA860 are close to the actual (derived) results.
- The bandwidth of this amplifier is very wide.

For the purpose of experiment, the transistor model of VDCC shown in Fig. 3 has been used along with some external circuitry. To explore the validity of the hardware arrangements, only the results of a sinusoidal oscillator are shown. It is worth noting that a resistor of 100 Ω, in series with the base of each diamond transistor and in series with input of the buffer of OPA860, is added [54]. For the realisation of hardware circuit, two Keysight programmable DC power supplies (E3632A) and a Caddo 30 MHz, 2-channel 4-trace Cathode Ray Oscilloscope (CRO) are used. The passive element values for the proper

functionality of the sinusoidal oscillator were chosen as $C_1 = C_2 = 470$ pF, $R_{M1} = 1/g_{m1} = 330\ \Omega$, $R_{M3} = 1/g_{m3} = 0 - 1$ kΩ and $R_2 = 330\ \Omega$. The actual hardwired implementation for the sinusoidal oscillator is shown in Fig. 23.

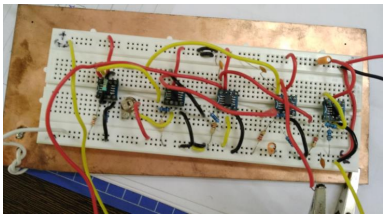

Fig. 23: Bread-board interconnection of the circuit.

The oscillator was ideally designed at 1 MHz and the corresponding simulations (using OPA860) were achieved at 940.2 kHz (giving an error of 5.8 %) and the hardware results were obtained at 910 kHz (giving an error of 9 % with respect to the ideal designed frequency). The complete range of the oscillator has also been tested for the designed hardware framework. Figure 24 shows the quadrature output, displayed on the CRO screen. Figure 25 shows the graph between the frequency of oscillation with respect to the variation in resistance value.

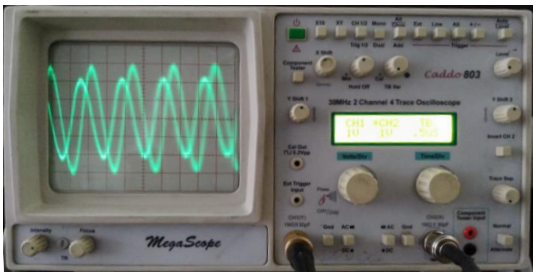

Fig. 24: Quadrature outputs.

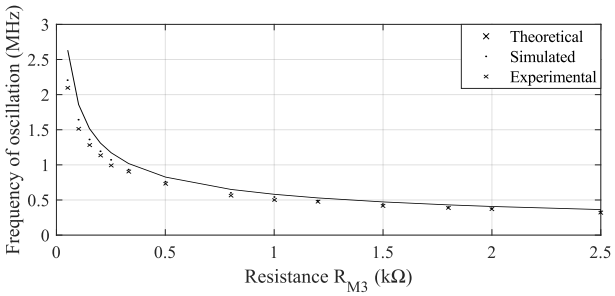

Fig. 25: FO with respect to RM3 (or g_3) using OPA 860.

7. Conclusion

The prime focus of this research article was to design a quadrature sinusoidal oscillator utilising only grounded passive elements and VDCC as an active element. The derived circuit offers quadrature outputs in current as well as voltage mode. The same circuit can be rearranged as an active filter by altering the position of the passive switches. The unique feature of the active filter is its impedance matching at the input and output port for making a higher-order current-mode filter. Regular mathematical calculations along with simulation results have also been included in the manuscript. At last, the experimental justification of the designed current-mode oscillator was also presented.

Acknowledgment

The experimental work was performed at Analog Electronics Lab of the department of Electronics Engineering, National Institute of Technology, Uttarakhand (Srinagar), Uttarakhand (India).

Author Contributions

M.G. conceived of the presented idea. T.S.A. developed the theory and S.N.G. performed the simulations and computations. T.S.A. and M.G. verified the analytical methods. T.S.A. carried out all the experimental work. T.S.A. and M.G. were in charge of overall direction and planning. T.S.A. wrote the manuscript with input from all authors. T.S.A., M.G. and S.N.G. discussed the results and contributed to the final manuscript.

References

[1] SENANI, R., D. R. BHASKAR, A. K. SINGH and V. K. SINGH. *Current Feedback Operational Amplifiers and Their Applications*. 1st ed. New York: Springer, 2013. ISBN 978-1-4614-5188-4.

[2] SENANI, R., D. R. BHASKAR, V. K. SINGH and R. K. SHARMA. *Sinusoidal Oscillators and Waveform Generators using Modern Electronic Circuit Building Blocks*. 1st ed. Cham: Springer, 2016. ISBN 978-3-319-23712-1.

[3] ARORA, T. S. and R. K. SHARMA. An All-Mode KHN Equivalent Biquad Using Third Generation Current Conveyor and All Grounded Passive Elements. *Proceedings of the National Academy of Sciences, India Section A: Physical Sciences*. 2017, vol. 87, iss. 1, pp. 97–108. ISSN 0369-8203, 2250-1762. DOI: 10.1007/s40010-016-0310-0.

[4] ARORA, T. S. and R. K. SHARMA. A Novel Cubic Generator Realised by CCIII-based Four

Quadrant Analog Multiplier and Divider. *Indian Journal of Science and Technology*. 2016, vol. 9, iss. 38, pp. 1–8. ISSN 0974-5645. DOI: 10.17485/ijst/2016/v9i38/100026.

[5] GUPTA, M. New Single Input Multiple Output Type Current Mode Biquad Filter Using OTAs. *Circuits and Systems*. 2016, vol. 7, iss. 4, pp. 231–238. ISSN 2153-1285. DOI: 10.4236/cs.2016.74022.

[6] SENANI, R., D. R. BHASKAR, M. GUPTA and A. K. SINGH. Canonic OTA-C Sinusoidal Oscillators: Generation of New Grounded-Capacitor Versions. *American Journal of Electrical and Electronic Engineering*. 2015, vol. 3, iss. 6, pp. 137–146. DOI: 10.12691/ajeee-3-6-2.

[7] ARORA, T. S. and S. GUPTA. A new voltage mode quadrature oscillator using grounded capacitors: An application of CDBA. *Engineering Science and Technology, an International Journal*. 2018, vol. 21, iss. 1, pp. 43–49. ISSN 2215-0986. DOI: 10.1016/j.jestch.2018.01.006.

[8] CHIEN, H.-C. Voltage- and Current-Modes Sinusoidal Oscillator Using a Single Differential Voltage Current Conveyor. *Journal of Applied science and Engineering*. 2013, vol. 16, iss. 4, pp. 395–404. ISSN 2708-9975. DOI: 10.6180/jase.2013.16.4.07.

[9] JIN, J. and C. WANG. Single CDTA-based current-mode quadrature oscillator. *AEU - International Journal of Electronics and Communications*. 2012, vol. 66, iss. 11, pp. 933–936. ISSN 1434-8411. DOI: 10.1016/j.aeue.2012.03.018.

[10] CHIEN, H.-C. and C.-Y. CHEN. CMOS realization of single-resistance-controlled and variable frequency dual-mode sinusoidal oscillators employing a single DVCCTA with all-grounded passive components. *Microelectronics Journal*. 2014, vol. 45, iss. 2, pp. 226–238. ISSN 0026-2692. DOI: 10.1016/j.mejo.2013.11.007.

[11] HORNG, J.-W., C.-L. HOU, C.-M. CHANG, W.-Y. CHUNG and H.-W. TANG. Current-Mode Multifunction Filters and Quadrature Oscillator Using Unit Gain Cells. *Journal of Active and Passive Electronic Devices*. 2006, vol. 1, iss. 1, pp. 247–258.

[12] KUMNGERN, M. and K. DEJHAN. DDCC-Based Quadrature Oscillator with Grounded Capacitors and Resistors. *Active and Passive Electronic Components*. 2009, vol. 2009, iss. 1, pp. 1–4. ISSN 1563-5031. DOI: 10.1155/2009/987304.

[13] TANGSRIRAT, W., P. MONGKOLWAI and T. PUKKALANUN. Current-mode high-Q bandpass filter and mixed-mode quadrature oscillator using ZC-CFTAs and grounded capacitors. *Indian Journal of Pure & Applied Physics*. 2012, vol. 50, iss. 1, pp. 600–607. ISSN 0975-1041.

[14] BIOLEK, D., R. SENANI, V. BIOLKOVA and Z. KOLKA. Active Elements for Analog Signal Processing: Classification, Review, and New Proposals. *Radioengineering*. 2008, vol. 17, iss. 4, pp. 15–32. ISSN 1210-2512.

[15] PRASAD, D., D. R. BHASKAR and M. SRIVASTAVA. New Single VDCC-based Explicit Current- Mode SRCO Employing All Grounded Passive Components. *Electronics*. 2014, vol. 18, iss. 2, pp. 81–88. ISSN 1450-5843. DOI: 10.7251/ELS1418081P.

[16] SOTNER, R., J. JERABEK, J. PETRZELA, N. HERENCSAR, R. PROKOP and K. VRBA. Second-Order Simple Multiphase Oscillator Using Z-Copy Controlled-Gain Voltage Differencing Current Conveyor. *Elektronika ir Elektrotechnika*. 2014, vol. 20, iss. 9, pp. 13–18. ISSN 2029-5731. DOI: 10.5755/j01.eee.20.9.8709.

[17] SOTNER, R., J. JERABEK, R. PROKOP and V. KLEDROWETZ. Simple CMOS voltage differencing current conveyor-based electronically tunable quadrature oscillator. *Electronics Letters*. 2016, vol. 52, iss. 12, pp. 1016–1018. ISSN 1350-911X. DOI: 10.1049/el.2016.0935.

[18] SRIVASTAVA, M. and D. PRASAD. VDCC Based Dual-Mode Quadrature Sinusoidal Oscillator with Outputs at Appropriate Impedance Levels. *Advances in Electrical and Electronic Engineering*. 2016, vol. 14, iss. 2, pp. 168–177. ISSN 1804-3119. DOI: 10.15598/aeee.v14i2.1611.

[19] GUPTA, M. and T. S. ARORA. Realization of Current Mode Universal Filter and a Dual-Mode Single Resistance Controlled Quadrature Oscillator Employing VDCC and Only Grounded Passive Elements. *Advances in Electrical and Electronic Engineering*. 2018, vol. 15, iss. 5, pp. 833–845. ISSN 1804-3119. DOI: 10.15598/aeee.v15i5.2397.

[20] MALIK, H., S. SRIVASTAVA, Y. R. SOOD and A. AHMAD. *Applications of Artificial Intelligence Techniques in Engineering*. 1st ed. Singapore: Springer, 2018. ISBN 978-981-13-1819-1.

[21] KACAR, F., A. YESIL and K. GURKAN. Design and experiment of VDCC-based voltage mode universal filter. *Indian Journal of Pure & Applied Physics*. 2015, vol. 53, iss. 5, pp. 341–349.

[22] KACAR, F., A. YESIL, S. MINAEI and H. KUNTMAN. Positive/negative lossy/lossless

grounded inductance simulators employing single VDCC and only two passive elements. *AEU - International Journal of Electronics and Communications*. 2014, vol. 68, iss. 1, pp. 73–78. ISSN 1434-8411. DOI: 10.1016/j.aeue.2013.08.020.

[23] ARORA, T. S., B. ROHIL and S. GUPTA. Fully Integrable/Cascadable CM Universal Filter and CM Quadrature Oscillator Using VDCC and Only Grounded Passive Elements. *Journal of Circuits, Systems and Computers*. 2019, vol. 28, iss. 11, pp. 1–36. ISSN 1793-6454. DOI: 10.1142/S0218126619501810.

[24] GUPTA, M., P. DOGRA and T. S. ARORA. Novel current mode universal filter and dual-mode quadrature oscillator using VDCC and all grounded passive elements. *Australian Journal of Electrical and Electronics Engineering*. 2019, vol. 16, iss. 4, pp. 220–236. ISSN 2205-362X. DOI: 10.1080/1448837X.2019.1648134.

[25] GUPTA, M. and T. S. ARORA. Various applications of analog signal processing employing voltage differencing current conveyor and only grounded passive elements: a re-convertible approach. *SN Applied Sciences*. 2020, vol. 2, iss. 9, pp. 1–18. ISSN 2523-3971. DOI: 10.1007/s42452-020-03379-6.

[26] ARORA, T. S. VDCC Based Sinusoidal Oscillators Using All Grounded Capacitors: A Series of Realization. *Wireless Personal Communications*. 2021, vol. 116, iss. 1, pp. 383–409. ISSN 1572-834X. DOI: 10.1007/s11277-020-07720-5.

[27] ARORA, T. S. A Current-Mode Single-Resistance-Controlled Oscillator Employing VDCC and All Grounded Passive Elements. *Iranian Journal of Electrical and Electronic Engineering*. 2020, vol. 16, iss. 2, pp. 184–191. DOI: 10.22068/IJEEE.16.2.184.

[28] BIOLEK, D., A. U. KESKIN and V. BIOLKOVA. Grounded capacitor current mode single resistance-controlled oscillator using single modified current differencing transconductance amplifier. *IET Circuits, Devices & Systems*. 2010, vol. 4, iss. 6, pp. 496. ISSN 1751-858X. DOI: 10.1049/iet-cds.2009.0330.

[29] LAHIRI, A. New realizations of voltage-mode quadrature oscillators using current differencing buffered amplifiers. *Journal of Circuits, Systems and Computers*. 2010, vol. 19, iss. 5, pp. 1069–1076. ISSN 1793-6454. DOI: 10.1142/S0218126610006608.

[30] HORNG, J.-W., Z.-R. WANG and T.-Y. YANG. Single ICCII Sinusoidal Oscillators Employing Grounded Capacitors. *Radioengineering*. 2011, vol. 20, iss. 3, pp. 608–613. ISSN 1805-9600.

[31] LAHIRI, A. Current-mode variable frequency quadrature sinusoidal oscillators using two CCs and four passive components including grounded capacitors. *Analog Integrated Circuits and Signal Processing*. 2012, vol. 71, iss. 2, pp. 303–311. ISSN 1573-1979. DOI: 10.1007/s10470-010-9571-8.

[32] SOTNER, R., J. JERABEK, N. HERENCSAR, Z. HRUBOS, T. DOSTAL and K. VRBA. Study of Adjustable Gains for Control of Oscillation Frequency and Oscillation Condition in 3R-2C Oscillator. *Radioengineering*. 2012, vol. 21, iss. 1, pp. 392–402. ISSN 1805-9600.

[33] PUSHKAR, K. L., D. R. BHASKAR and D. PRASAD. Single-Resistance-Controlled Sinusoidal Oscillator Using Single VD-DIBA. *Active and Passive Electronic Components*. 2013, vol. 2013, iss. 1, pp. 1–5. ISSN 1563-5031. DOI: 10.1155/2013/971936.

[34] MAHESHWARI, S. Voltage-Mode Four-Phase Sinusoidal Generator and Its Useful Extensions. *Active and Passive Electronic Components*. 2013, vol. 2013, iss. 1, pp. 1–8. ISSN 1563-5031. DOI: 10.1155/2013/685939.

[35] BHASKAR, D. R., D. PRASAD and K. L. PUSHKAR. Fully Uncoupled Electronically Controllable Sinusoidal Oscillator Employing VD-DIBAs. *Circuits and Systems*. 2013, vol. 4, iss. 3, pp. 264–268. ISSN 2153-1293. DOI: 10.4236/cs.2013.43035.

[36] JIN, J. and C. WANG. CDTA-based electronically tunable current-mode quadrature oscillator. *International Journal of Electronics*. 2014, vol. 101, iss. 8, pp. 1086–1095. ISSN 1362-3060. DOI: 10.1080/00207217.2013.805394.

[37] YUCEL, F. and E. YUCE. CCII based more tunable voltage-mode all-pass filters and their quadrature oscillator applications. *AEU - International Journal of Electronics and Communications*. 2014, vol. 68, iss. 1, pp. 1–9. ISSN 1434-8411. DOI: 10.1016/j.aeue.2013.06.012.

[38] HORNG, J.-W., C.-L. HOU, C.-M. CHANG, S.-T. CHENG and H.-Y. SU. Current Or/And Voltage-Mode Quadrature Oscillators with Grounded Capacitors and Resistors using FD-CCIIs. *WSEAS Transactions on Circuits and Systems*. 2008, vol. 7, iss. 3, pp. 129–138. ISSN 1109-2734.

[39] LAHIRI, A., W. JAIKLA and M. SIRIPRUCHYANUN. Voltage-mode quadrature sinusoidal oscillator with current tunable properties. *Analog Integrated Circuits and Signal Processing*. 2010, vol. 65, iss. 2, pp. 321–325. ISSN 1573-1979. DOI: 10.1007/s10470-010-9488-2.

[40] SOTNER, R., Z. HRUBOS, J. SLEZAK and T. DOSTAL. Simply Adjustable Sinusoidal Oscillator Based on Negative Three-Port Current Conveyors. *Radioengineering*. 2010, vol. 19, iss. 3, pp. 446–454. ISSN 1805-9600.

[41] MAHESHWARI, S. and B. CHATURVEDI. High output impedance CMQOs using DVCCs and grounded components. *International Journal of Circuit Theory and Applications*. 2011, vol. 39, iss. 4, pp. 427–435. ISSN 0098-9886. DOI: 10.1002/cta.636.

[42] ABDALLA, K. K., D. R. BHASKAR and R. SENANI. Configuration for realising a current-mode universal filter and dual-mode quadrature single resistor controlled oscillator. *IET Circuits, Devices & Systems*. 2012, vol. 6, iss. 3, pp. 1–9. ISSN 1751-8598. DOI: 10.1049/iet-cds.2011.0160.

[43] LAHIRI, A. Deriving (MO)(I)CCCII Based Second-order Sinusoidal Oscillators with Non-interactive Tuning Laws using State Variable Method. *Radioengineering*. 2011, vol. 20, iss. 1, pp. 349–353. ISSN 1805-9600.

[44] JIN, J. Current-Mode Resistorless Simo Universal Filter And Four-Phase Quadrature Oscillator. 2014, vol. 7, iss. 2, pp. 1–6. DOI: 10.5281/ZENODO.1335982.

[45] LI, Y. A. Electronically tunable current-mode biquadratic filter and four-phase quadrature oscillator. *Microelectronics Journal*. 2014, vol. 45, iss. 3, pp. 330–335. ISSN 0026-2692. DOI: 10.1016/j.mejo.2013.12.005.

[46] SUMMART, S., C. THONGSOPA and W. JAIKLA. New current-controlled current-mode sinusoidal quadrature oscillators using CDTAs. *AEU - International Journal of Electronics and Communications*. 2015, vol. 69, iss. 1, pp. 62–68. ISSN 1434-8411. DOI: 10.1016/j.aeue.2014.07.011.

[47] KUMNGERN, M., P. LAMUN and K. DEJHAN. Current-mode quadrature oscillator using current differencing transconductance amplifiers. *International Journal of Electronics*. 2012, vol. 99, iss. 7, pp. 971–986. ISSN 1362-3060. DOI: 10.1080/00207217.2011.651693.

[48] MINAEI, S. and E. YUCE. Novel Voltage-Mode All-Pass Filter Based on Using DVCCs. *Circuits, Systems and Signal Processing*. 2010, vol. 29, iss. 3, pp. 391–402. ISSN 1531-5878. DOI: 10.1007/s00034-010-9150-3.

[49] SOTNER, R., J. JERABEK, R. PROKOP and K. VRBA. Current Gain Controlled CCTA and its Application in Quadrature Oscillator and Direct Frequency Modulator. *Radioengineering*. 2011, vol. 20, iss. 1, pp. 317–326. ISSN 1805-9600.

[50] SOTNER, R., Z. HRUBOS, N. HERENCSAR, J. JERABEK, T. DOSTAL and K. VRBA. Precise Electronically Adjustable Oscillator Suitable for Quadrature Signal Generation Employing Active Elements with Current and Voltage Gain Control. *Circuits, Systems, and Signal Processing*. 2014, vol. 33, iss. 1, pp. 1–35. ISSN 1531-5878. DOI: 10.1007/s00034-013-9623-2.

[51] SOTNER, R., J. JERABEK, N. HERENCSAR, J. PETRZELA, K. VRBA and Z. KINCL. Linearly tunable quadrature oscillator derived from LC Colpitts structure using voltage differencing transconductance amplifier and adjustable current amplifier. *Analog Integrated Circuits and Signal Processing*. 2014, vol. 81, iss. 1, pp. 121–136. ISSN 1573-1979. DOI: 10.1007/s10470-014-0353-6.

[52] SOTNER, R., J. JERABEK, L. LANGHAMMER, J. POLAK, N. HERENCSAR, R. PROKOP, J. PETRZELA and W. JAIKLA. Comparison of Two Solutions of Quadrature Oscillators With Linear Control of Frequency of Oscillation Employing Modern Commercially Available Devices. *Circuits, Systems, and Signal Processing*. 2015, vol. 34, iss. 11, pp. 3449–3469. ISSN 1531-5878. DOI: 10.1007/s00034-015-0015-7.

[53] SATIPAR, D., P. INTANI and W. JAIKLA. Electronically Tunable Quadrature Sinusoidal Oscillator with Equal Output Amplitudes during Frequency Tuning Process. *Journal of Electrical and Computer Engineering*. 2017, vol. 2017, iss. 1, pp. 1–10. ISSN 2090-0155. DOI: 10.1155/2017/8575743.

[54] Wide Bandwidth Operational Transconductance Amplifier (OTA) and Buffer. In: *Texas Instruments* [online]. 2008. Available at: `https://www.ti.com/lit/ds/symlink/opa860.pdf?ts=1628152082082&ref_url=https%253A%252F%252Fwww.google.com%252`.

About Authors

Tajinder Singh ARORA (Senior Member, IEEE) was born 1979 in Dehradun, Uttarakhand, India. He has completed his B.Tech. (Electronics and Communication Engineering) from C.C.S.University in 2002, M.Tech. (Signal Processing) from Netaji Subhas Institute of Technology, New Delhi in 2008, Ph.D. (Analog Signal Processing) from Uttarakhand Technical University, Dehradun in 2017. He is currently working as an Assistant Professor with Department of Electronics Engineering, National Institute of Technology, Uttarakhand, India. His research interests are in the area of current mode signal processing, electronic circuit design, electronic devices etc. He has authored or co-authored 25 research papers in International Journals and Conferences.

Manish GUPTA was born 1975 in Ghaziabad, Uttar Pradesh, India. He obtained B.Tech Degree in Electronics and Communication Engineering from Delhi College of Engineering, Delhi, (presently D.T.U. Delhi), M.Tech with specialization in Signal Processing from Netaji Subhas Institute of Technology, New Delhi and Ph.D. in area of Analog Integrated Circuits and Signal Processing from Jamia Millia Islamia, New Delhi, India. Currently he is working as an Associate Professor with Department of Electronics and Communication Engineering, Inderprastha Engineering College, Ghaziabad, Uttar Pradesh, India. His research interests are in the area of Bi-polar and CMOS, analog integrated circuits, current-mode signal processing.

Shiv Narain GUPTA was born 1982 in Jaunpur, Uttar Pradesh, India. He has completed his B.Tech degree in Electronics and Communication Engineering from Uttar Pradesh Technical University in 2006 and M.Tech degree in Digital Communication from Ambedkar Institute of Technology, Delhi in 2009. He is pursuing Ph.D. from Jaypee Institute of Information Technology (JIIT), Noida. His research areas are analog integrated circuits and analog signal processing applications.