Reducing the Source Resistance by Increasing the Gate Effect on Substrate for Future Terahertz HEMT Devices

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Abstract. *In this paper, we present the dependence of source resistance sensibility on the gate bias effect in a High Electron Mobility Transistor (HEMT) using the Drift-Diffus (D-D) model with the SILVACO Technology Computer-Aided Design (TCAD) tool. The obtained results show that the increases of gate bias effect on substrate lead to decreasing the source resistance of the simulated device. The reported increase in the effect of gate induces the increases of transferred holes concentration towards the source region and which induce the decreases of source resistance. The decrease of source resistance can also be made by reducing the buffer thickness which leads to an increase in the gate effect on the substrate. The source resistance value is influenced by the Drain-Induced Barrier Lowering (DIBL) effect where the rate of decreasing the source resistance will be decreasing consequently to increase the drain bias. The reduction of the source resistance induces the increase of device sensibility for lows values of current.*

Keywords

Device performances, gate effect, High Electron Mobility Transistors (HEMT), hole concentration, source resistance, substrate.

1. Introduction

Recently, High Electron Mobility Transistor (HEMT) or Heterojunction Field Effect Transistors are important element for devices that operate in the terahertz range, and power electronics applications [1], [2] and [3]. This family of devices can handle high power and can work efficiently at high temperatures [4]. One of the main consequences that induce this technological progress is the proceeding device scaling which reached the nano-order [5] and [6], Therefore, this it can be deployed to the terahertz monolithic integrated circuits based on different transistor technologies in the submillimeter-wave frequency regime [7]. Also, high-speed, high breakdown voltage transistors are required in future systems and application where the InP-HEMTs have to find a place, mainly where the channel material is well-chosen [8] and [9]. Many studies and structures are developed for this technology covering all areas and fields of electronics [9], [10], [11], [12], [13] and [14], recently it is the preferred technology for low-power and high-speed applications due to high operating frequency reaching the terahertz range [15], [16] and [17]. On the other hand, the InP-HEMTs are recommended due to the channel properties, mainly the electronic transport properties. In the case of fast devices the use of $In_{0.53}Ga_{0.47}As$ [18] or their derived materials such as $In_{0.7}Ga_{0.3}As$ [19], $In_{0.75}Ga_{0.25}As$ [20], and InAs is the best solution to this objective [21] and [22]. It is necessary to report that not only the transistor has to be scaled for reaching the higher frequencies, but also the decreases of parasites effect and the use of new materials such as substrate material [23], [24], [25], [26] and [27]. In this paper, we present a new concept that can significantly decrease the source resistance which induces the increase of device frequency and current sensibility. The proposed concept is based on the principle of increasing the gate bias effect on the substrate by reducing their structural energy

or the buffer layer thickness. Consequently, a significant increase of accumulated hole concentration occurs under the source region, decreasing the source resistance.

2. Device Structure

In this work, we present the performance of HEMT with 30 nm gate length based on $InAs_{0.3}P_{0.7}$ in its substrate. The cross-sectional view of the simulated structure is shown in Fig. 1. The structure consists of 5,000 nm of a semi-insulating $InAs_{0.3}P_{0.7}$ substrate, which allows presenting our objective, and 300 nm intrinsic $In_{0.52}Al_{0.48}As$ buffer layer which is necessary to isolate the composite channel from the substrate defects. The composite channel is formed by 5 nm of intrinsic InAs for the core channel, 3 nm, and 2 nm of intrinsic $In_{0.7}Ga_{0.3}As$ for the lower sub-channel and upper sub-channel, respectively. The Schottky barrier layer is about 11 nm, but it was reduced under the gate to about 2 nm. This barrier is formed by the intrinsic $In_{0.52}Al_{0.48}As$ to enhance the frequency performance. The 30 nm $InAs_{0.3}P_{0.7}$ substrates were used only for Si δ-doping level with 1 nm thickness ($5 \cdot 10^{12}$ cm^{-3}) that it is necessarily used to increase the sheet charge density in the composite channel that turns an increase in the g_m and drain current. The spacer for this structure is about 2 nm formed by $In_{0.52}Al_{0.48}As$. 6 nm thick InP etch stop layer is crossed to minimize the access of resistance for both regions of source and drain electrodes. In our structure, we use a heavily doped multilayer cap formed with three levels; the first is 5 nm thick $In_{0.7}Ga_{0.3}As$ upper layer ($1 \cdot 10^{18}$ cm^{-3}), the second is 10 nm thick $In_{0.53}Ga_{0.47}As$ layer ($1 \cdot 10^{18}$ cm^{-3}) and the third is 5 nm of the intrinsic $In_{0.52}Al_{0.48}As$ layer.

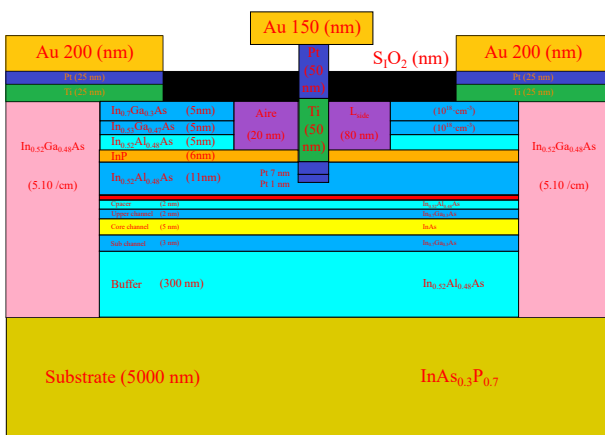**Fig. 1:** Structure of proposed $InAs_{0.3}P_{0.7}$ based HEMT.

The source and drain ohmic contacts were formed using Ti/Pt/Au (25 nm/25 nm/150 nm) metal stack and the T-gate was formed by Pt/Ti/Pt/Au (7 nm/50 nm/50 nm/150 nm) metal stack. More-over, the gate used a buried 1 nm thin platinum metal layer to reduce the short channel effects in the formed device. It helps to effectively reduce the thickness of the Schottky barrier layer to 1 nm, which in turn reduces the gate-to-channel separation. It enhances the velocity of electrons under the gate which helps to reduce the intrinsic delay and consequently, it increases the frequency performance of the device [28]. It induces a reduction in parasitic capacitances and resistances of the device compared to traditional recessed metal gate technology and it significantly reduces the kink effects in the output characteristics. Finally, a 60 nm thick SiO_2 layer was used for device passivation. With the objective to improve the device's performance, our structure presents 100 nm length for heavily doped ($5 \cdot 10^{19}$ cm^{-3}) $In_{0.52}Ga_{0.48}As$ in both regions as a source and drain. The following parameters were chosen: the gate length of 30 nm, the source-to-drain separation of 630 nm and the side recess spacing (L_{SIDE}) of 80 nm.
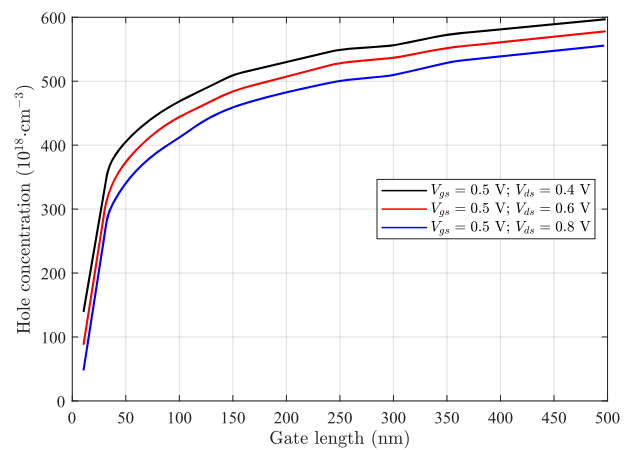
3. Results and Discussion

Fig. 2: Evolution of hole concentration under the source as a function of gate length under $V_{gs} = 0.5$ V.

Our simulation has been made with SILVACO Technology Computer-Aided Design (TCAD) at room temperature. This software serves to provide the characteristics of the proposed structure which takes into consideration the effect of the materials system used in the morphological description of the structure. The drift-diffuse model use is presented in [29]. We have chosen the gate length of 30 nm to decrease the short channel effect and the gate width $W = 2 \cdot 10$ μm. According to Fig. 2 for 30 nm substrate based on $InAs_{0.3}P_{0.7}$, the holes concentration under the source is about $350 \cdot 10^{18}$ cm^{-3}, $335 \cdot 10^{18}$ cm^{-3}, and $310 \cdot 10^{18}$ cm^{-3} for 0.5 V in gate voltage and 0.4 V, 0.6 V, 0.8 V in drain voltages, respectively. The improvements of holes concentration with increase

of the gate length to 300 nm are 60 %, 59 %, and 64 % respectively. They are $560 \cdot 10^{18}$ cm^{-3}, $535 \cdot 10^{18}$ cm^{-3} and $510 \cdot 10^{18}$ cm^{-3} due to increasing the field-effect with increasing the gate length which induces the increase in the affected holes concentration. Consequently, it significantly increases the transferred holes concentration from the substrate to the source. The increase of drain bias leads to degrading the field-effect for all gate lengths due to the short channel effect, as shown in Fig. 2. The increases in gate voltage induces the increase of transferred holes concentration due to increasing the applied electric field, as shown in Fig. 2 and Fig. 3.
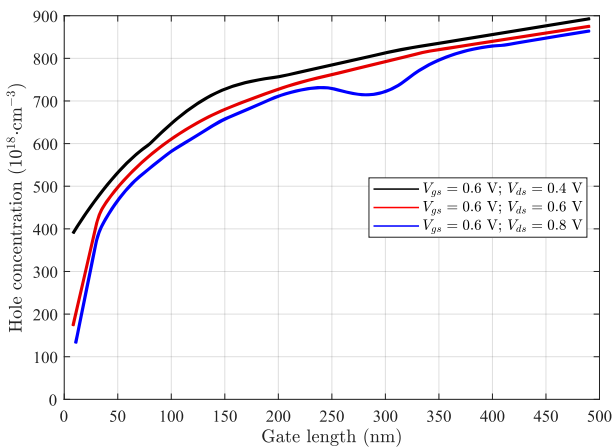

Fig. 3: Evolution of hole concentration under the source as a function of gate length under $V_{gs} = 0.6$ V.
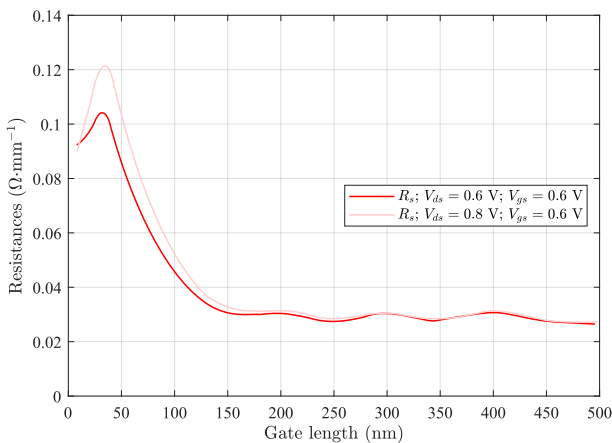

Fig. 4: R_s as a function of gate length under.

The improvement of holes concentration under the source region improves the source resistance for all gate lengths of the proposed structure, as shown in Fig. 4. The evolution of R_s can be divided into two parts above and below 30 nm of the gate length. First, with increase of the gate length, R_s decreases until 0.03 $\Omega \cdot$mm^{-1} for $L_g = 500$ nm. However, in the case of $L_g = 30$ nm, R_s is about 0.105 $\Omega \cdot$mm^{-1} and presents an increase of 19 % with increasing V_{ds} to 0.8 V where it reaches 0.125 $\Omega \cdot$mm^{-1} due to de-

creasing of the affected holes concentration in the substrate. Consequently, the reduction value of gate bias with increases drain bias (DIBL effect) is induced. Below 30 nm the record decreasing in R_s with the decreasing gate length is attributed to the short channel effect. The proposed structure with 30 nm gate length, heavily doped source and drain regions, and single Si δ-doping level with $N_d = 5 \cdot 10^{12}$ cm^{-3} have exhibited g_m of about 7,000 mS$\cdot$mm^{-1} for $V_{ds} = 0.1$ V, and 9,000 mS$\cdot$mm^{-1} for $V_{ds} = 0.6$ V. This is due to the best conditions of confinement caused by the spacer/channel barrier where it increases with the increasing of drain bias, as shown in Fig. 5
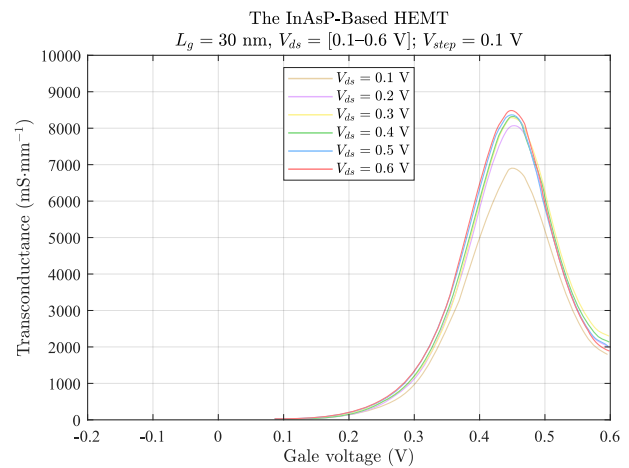

Fig. 5: The transconductance in the InAs$_{0.3}$P$_{0.7}$ based HEMT.
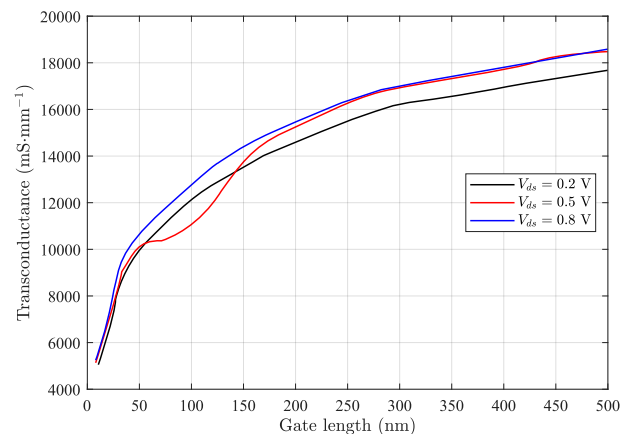

Fig. 6: The transconductance g_m as a function of the gate length.

Similar to their behavior as a function of gate length of 30 nm the proposed structure reaches 8,468 mS$\cdot$mm^{-1}, 8,795 mS$\cdot$mm^{-1}, and 9,166 mS$\cdot$mm^{-1} in their transconductances gm under 0.2 V, 0.5 V, and 0.8 V of drain bias respectively. It presents 83 %, 85 %, and 77 % of improvement, respectively. When L_g is increased to 300 nm, g_m become 15,580 mS$\cdot$mm^{-1}, 16,347 mS$\cdot$mm^{-1} and 16,265 mS$\cdot$mm^{-1}, as shown in Fig. 6. The proposed structure with the gate length

of 60 nm and 85 nm under $V_{ds} = 0.5$ V showed better improvement compared to other references and under the same conditions as [31], [32] and [32]. All these enhancements in the transconductance are attributed to the decreases related to source resistance and reduction of short channel effect.

The simulated structure with 30 nm in gate length exhibits 1.6 THz and 7.2 THz in F_t and F_c, respectively, under $V_{ds} = 0.6$ V. It showed an improvement of 11 % and 56 % when V_{ds} increased to 0.8 V where both frequencies F_t and F_c reached 2.5 THz and 8 THz, respectively, as shown in Fig. 7 and Fig. 8. Similar to the 300 nm gate length, F_t and F_c are 0.6 THz and 0.14 THz for $V_{ds} = 0.6$ V and they reached 0.65 THz, 0.145 THz when V_{ds} increased to 0.8 V. This high frequency for both frequency characteristics is due to the use of InAs$_{0.3}$P$_{0.7}$ as substrate material which can significantly decreases the source resistance which in turn increases the device transconductance. The increase in the gate length induces a decrease in the frequency characteristics which describe the device, as shown in Fig. 9. It is distributed to the increase of time transition and the distance between the source and drain.
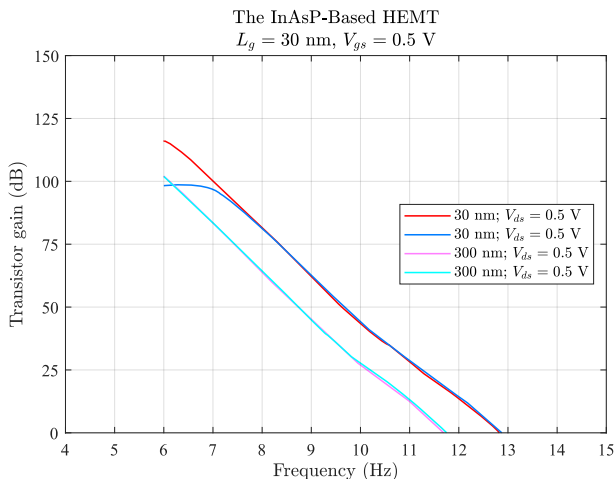

Fig. 7: Cut-off frequency F_c of proposed InAs$_{0.3}$P$_{0.7}$ based HEMT.

For all gate lengths, the proposed structure based on the InAs$_{0.3}$P$_{0.7}$ substrate with $W = 2 \cdot 10$ µm and heavily doped source and drain regions has shown the best behavior in frequency mode compared to other references. For 15 nm gate length, it presents 8.5 THz and 3.1 THz under $V_{ds} = 0.6$ V for F_c and F_t, respectively, as shown in Fig. 9. They showed 5 times and 27 times greater values than in [33], where they reached 610 GHz and 305 GHz, respectively. Similarly 20 nm gate length showed 5.03 times and 7 times greater values of F_t and F_c compared to [28], and 5.67 times and 9 times greater compared to [34]. F_t and F_c for the proposed structure are 4.2 THz and 9.5 THz respectively under $V_{ds} = 0.6$ V, 834 GHz and 1,200 GHz, respectively,
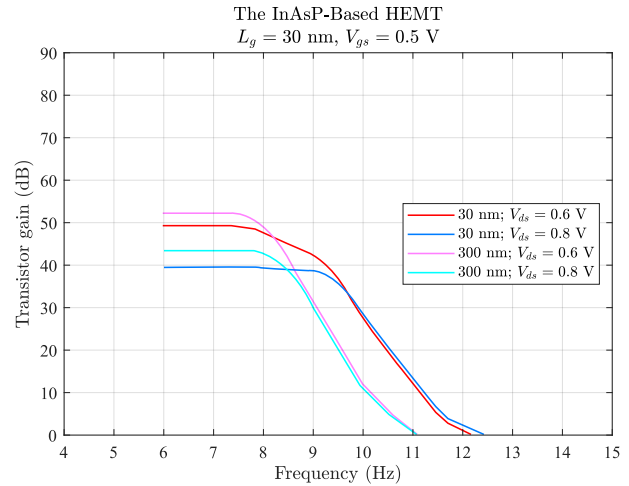

Fig. 8: The transition frequency F_t of proposed InAs$_{0.3}$P$_{0.7}$ based HEMT.
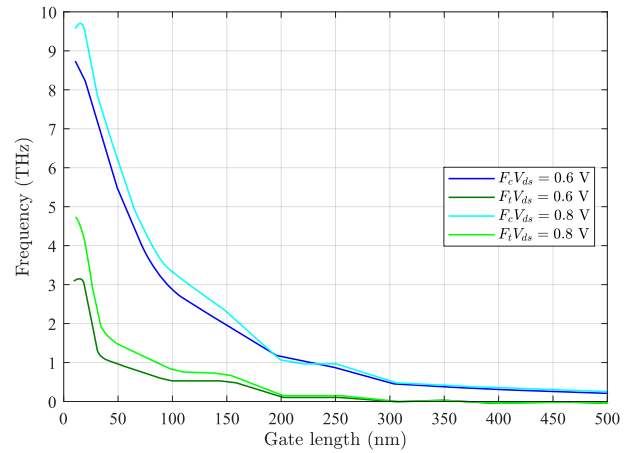

Fig. 9: F_c and F_t as a function of gate length for proposed InAs$_{0.3}$P$_{0.7}$ based HEMT.

under $V_{ds} = 1$ V [28], and 740 GHz and 1,040 GHz, respectively, under $V_{ds} = 0.8$ V [34]. For $L_g = 30$ nm and the proposed structure based on InAs$_{0.3}$P$_{0.7}$ substrate, F_c and F_t reached 2.5 THz and 8 THz, respectively, under $V_{ds} = 0.8$ V, which means 4 times and 20 times greater values than in [35] where the values of 547 GHz and 400 GHz were reached under $V_{ds} = 0.9$ V. For $L_g = 100$ nm and the proposed structure based on InAs$_{0.3}$P$_{0.7}$ substrate, F_c and F_t reached 950 GHz and 3.4 THz, respectively, under $V_{ds} = 0.8$ V, i.e., 3 times and 8 times greater than in [36] where they reached 249 GHz and 415 GHz, respectively, under $V_{ds} = 1.8$ V. There are several advantages of both frequencies in our proposed structure compared to the other structures: (1) The increases in the transconductance is produced in the channel with the increase in the hole concentration under the source region which induces a considerable decrease in the source resistance. (2) The effect of the buried thin platinum metal layer leads to decreaseds distance from the gate to the composite channel. (3) We get a reduction in parasitic parameters

of the device. These frequency values for all gate lengths are the best and the highest ever reported among any E-mode HEMTs on any material substrate used and for any technology. The mobility of the electrons and holes in the proposed structure based on the $InAs_{0.3}P_{0.7}$ substrate under the gate region with 30 nm gate length reached about 24,480 $cm^2 \cdot V^{-1} \cdot S^{-1}$ and 367 $cm^2 \cdot V^{-1} \cdot S^{-1}$, respectively. The drift velocity reached $4.8 \cdot 10^8$ $cm \cdot s^{-1}$ and $8.5 \cdot 10^6$ $cm \cdot s^{-1}$ for the electrons and holes, respectively. This enhancement in mobility and velocity can justify the best frequency behavior that characterizes the proposed device. It is due to the decreases of input resistance with an increase of the holes concentration under the source region and the effect of the lattice strain introduced by the lattice mismatch between $In_{0.53}Ga_{0.47}As$ source and drain regions and the $In_{0.7}Ga_{0.3}As/InAs/In_{0.7}Ga_{0.3}As$ composite channel layers.
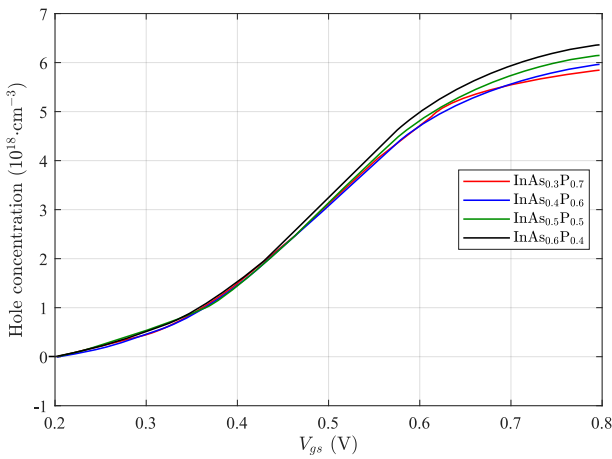
Fig. 10: Hole concentration as function of V_{gs} under $V_{ds} = 0.8$ V for $InAs_{0.3}P_{0.7}$, $InAs_{0.4}P_{0.6}$, $InAs_{0.5}P_{0.5}$, $InAs_{0.6}P_{0.4}$.

The calculated DIBL effect with its well-known law $\left(\text{DIBL} = \dfrac{\Delta V_{th}}{\Delta V_{ds}} \right)$ is about 13 mV·V^{-1} for the proposed structure based on $InAs_{0.3}P_{0.7}$ substrate and 30 nm gate length due to the high transconductance caused by reducing the source resistance and low separation distance between gate and 2DEG. This improvement in the resulting decrease of DIBL can justify the importance of decreasing the parasitic source resistance. On the other hand, it proves the better structural description of the proposed structure, mainly the best commendably of the channel without the drain bias effect (short channel). The increasing of arsenic mole fraction in the chemical composition of the substrate induces a significant increase in the holes concentration transferring towards the source region due to the high field in the substrate level produced by the gate bias. Consequently, decreasing of the substrate energy will be higher in the level where the field occurs. The hole concentration increases from $5.45 \cdot 10^{18}$ cm^{-3} in the case of 30 % arsenic molar fraction under 0.6 V for the gate

bias and 0.8 V for the drain bias to $5.52 \cdot 10^{18}$ cm^{-3} and $5.69 \cdot 10^{18}$ cm^{-3}, i.e., for 50 % and 60 % of molar fraction, respectively, and under the same bias values. For all mole fractions used in this study, the increases of drain bias induce the reduction of transferred holes concentration due to the DIBL effect, as shown in Fig. 10 and Fig. 11.
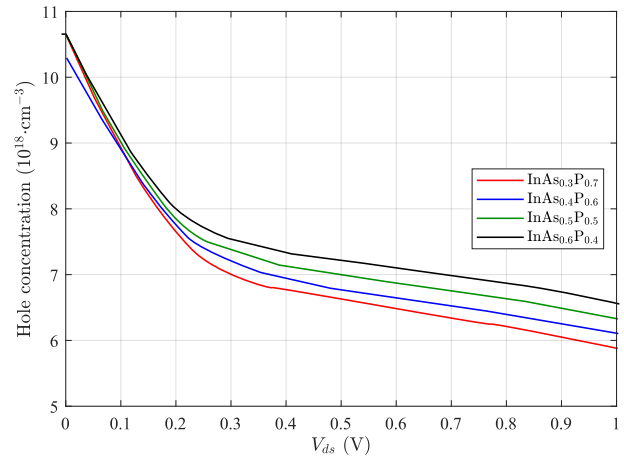

Fig. 11: Hole concentration as function of V_{ds} under $V_{gs} = 0.8$ V for $InAs_{0.3}P_{0.7}$, $InAs_{0.4}P_{0.6}$, $InAs_{0.5}P_{0.5}$, $InAs_{0.6}P_{0.4}$.
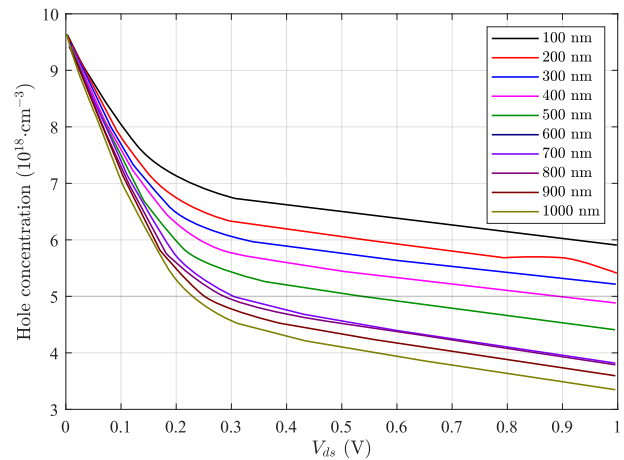
Fig. 12: Holes concentration as a function of V_{ds} under the effect of buffer thickness for $InAs_{0.3}P_{0.7}$.

The importance of increasing the field effect on the substrate can be presented as a function of buffer layer thickness. The obtained simulation results for a substrate based on $InAs_{0.3}P_{0.7}$ are shown in Fig. 12 and Fig. 13. The holes concentration increases with decreasing the buffer thickness due to increasing the field effect. The hole concentration is about $4.19 \cdot 10^{18}$ cm^{-3} for 900 nm in the thickness of the buffer layer, which presents an improvement of 11.69 % and 35.08 % when the buffer thickness is decreasing to 600 nm and 300 nm, respectively, so they are $4.68 \cdot 10^{18}$ cm^{-3} and $5.66 \cdot 10^{18}$ cm^{-3}, respectively, as shown in Fig. 12. In the same buffer thickness, the increases of V_{gs} in-

creases the hole concentration in contrast to V_{ds} where their increase makes a decrease in the holes concentration, as shown in Fig. 13. The registered improvement in hole concentration under the source region makes an important decrease in the source resistance. Consequently, it affects the set characteristics that describe the device.

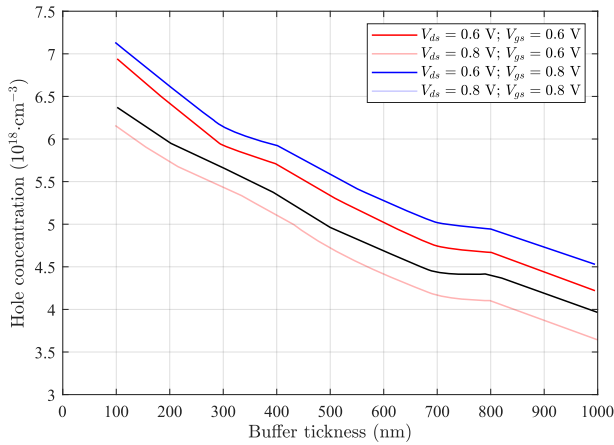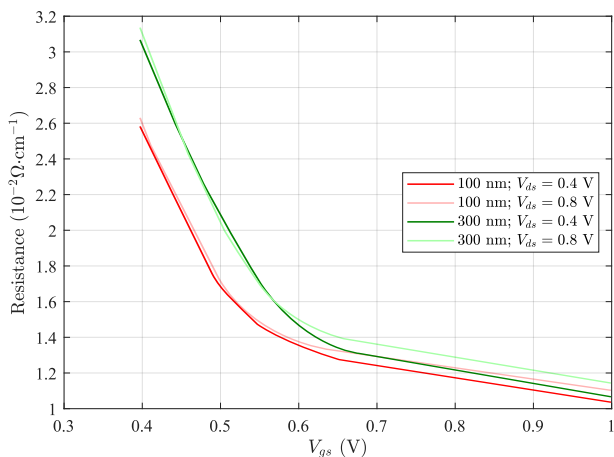**Fig. 13:** Holes concentration as a function of buffer thickness for $InAs_{0.3}P_{0.7}$.

Fig. 14: Source resistance as a function of V_{gs} under the effect of buffer thickness and V_{ds} in $InAs_{0.3}P_{0.7}$.

In both Fig. 14 and Fig. 15, we present the source resistance as a function of drain and gate biases under the effect of buffer layer thickness. Both figures shown that the decrease of buffer layer thickness induces the decrease of source resistance due to increasing the field effect on the substrate, where it will be intense. That means the gate bias effect on the substrate increase. The increases of source resistance under high values of drain bias (V_{ds}) is attributed to the DIBL effect. Comparing of Fig. 10 and Fig. 14 presents the source resistance sensibility as a function of the substrate energy through the transferred holes concentration. Also, it can be used to explain the gate bias effect on the source resistance when increase in the gate bias induces the decrease of source resistance,

which can be influenced by the DIBL effect with the increase of the drain bias.
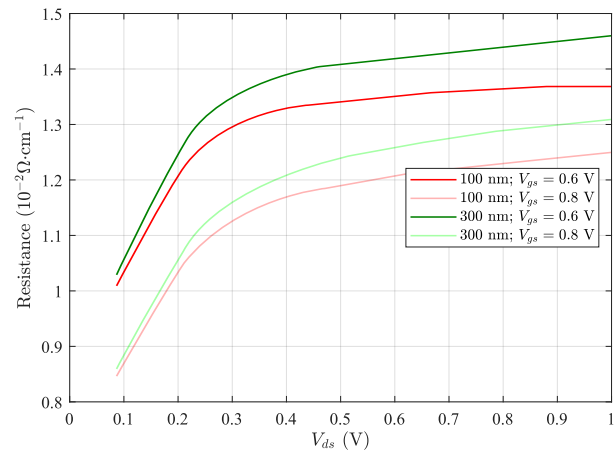

Fig. 15: Source resistance as a function of V_{ds} under the effect of buffer thickness and V_{gs} in $InAs_{0.3}P_{0.7}$.

4.   Conclusion

Our work consists of studying the reduction of source resistance by increasing the gate bias effect for a HEMT's technology using the TCAD SILVACO tool and Drift-Diffuse model. The main results obtained show that the increase of gate bias effect on the substrate induces the decreasing of source resistance also in the case of reducing the substrate structural energy. This, in turn, increases the transferred hole concentration accumulated under the source region. The source resistance value is influenced by the DIBL effect when the rate of decreasing the source resistance will be decreasing when the drain bias is increased. On the other hand, the source resistance decreases with the use of low buffer thickness due to the already increased gate effect. The optimal choice of its value is an important task for producing efficient devices. Increasing the V_{ds} induces an increase of cut-off and transition frequencies. The increase of the gate length induces the decrease of both studied frequency characteristics (cut-off and transition) due to the increase of time transition with the increase of the distance between the source and drain. The increase of gate effect on the substrate induces the increase in transferred hole concentration to the source region. Increasing the buffer layer thickness induces significant decrease in the transferred hole concentration to the source region which can decrease the source resistance considerably due to decreasing the gate effect on the substrate. The using of a substrate material that is characterized by low structural energy properties leads to the enhanced hole concentration transferred towards source region and, consequently, to increased effect of the applied electric field in the substrate. This causes a significant decrease in

the input resistance of the device which improves its frequency characteristics. The obtained low-resistance source is presented as an advantageous characteristic that allows producing the efficient devices, such as in our case the HEMT's, operating in low energy and characterized by low input current and voltage, mainly dedicated to the bio-engineering field.

Author Contributions

S.D. conceived of the presented idea, supervised this work and discussed the results, also S.D. contributed to the final manuscript (He wrote the manuscript to it final version). S.D. contributed to carry out the final morphological description to the proposed structure ender TCAD SILVACO software and implementing the proposed program. S.D. planned and carried out the simulations results and their final interpretation. S.D. verified the obtained results with the other similar results existing in the bibliography. S.D. carried out and preparing the published work, also he specified the critical review and answer to reviewers commentary including in publication stages.

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