Degradation Analysis of DC-Link Aluminium Electrolytic Capacitors Operating in PWM Power Converters

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Abstract. *The most common failure mode of aluminium electrolytic capacitor is the so-called wear out fault. It is caused by the high core temperature of the capacitor. Therefore, life cycle calculations generally use temperature data to estimate degradation level. Core temperature-based life cycle calculations can consider different current loads on capacitors. The calculation method uses scaling factors for different ripple current waveforms. However, it is not observed that temperature only is responsible for aging, but current waveform also influences the level of degradation. Therefore, sinusoidal and PWM-loaded capacitor tests were performed under the same temperature conditions. The results show that the pore distribution of aluminium anode foil has changed during the test. The pore diameter reduces and it leads to an increase in the ESR value and decrease in the capacitance, electrolyte amount and weight. Comparative results show that the PWM-loaded capacitor is more degraded than the capacitor loaded by sinusoidal test current.*

Keywords

Aluminium electrolytic capacitors, DC-link capacitor aging, pulse width modulated power converters.

1. Introduction

Aluminium electrolytic capacitors have been used almost in every power electronic system and application, such as Power Factor Correction (PFC) circuits, power supplies, PWM inverters or other switch-mode converters, because they have relatively high capacitance and low cost. The capacitor as an energy storage element is used as a voltage level compensator between input and output power levels to decrease the ripple of the DC-side voltage level.

The common faults in electrolytic capacitors during long-term usage or misapplication are wear-out faults [1], [2], [3], [4], [5], [6], [7], [20], [21] and [22] due to the vaporization of electrolyte caused by high core temperature. Inside the capacitor, there are continuous hydrolysis and oxide-layer forming mechanisms due to current flow through the anode foil (Fig. 1). The aluminium anode foil is oxidized by the oxygen from the water content of the electrolyte. The thicken oxide layer of the anode foil, the reducing electrolyte and the increasing hydrogen gas formation are the different appearances of the degradation.

The occurrence of degradation can be delayed and its level can be reduced if the operating temperature and the heat generated by the ripple current are lowered. The capacitor core temperature (T_C) is determined [8] by Eq. (1):

$$T_C = T_A + I_{C,rms}^2 R_{ESR} R_{th}, \tag{1}$$

where T_A denotes the ambient temperature, $I_{C,rms}$ symbolizes the capacitor RMS current, R_{ESR} denotes the equivalent serial resistance and R_{th} denotes the thermal resistance between the capacitor can and the environment. Decrease in the inner temperature of capacitor by 10 °C in the rated operating temperature doubles the capacitor lifespan.

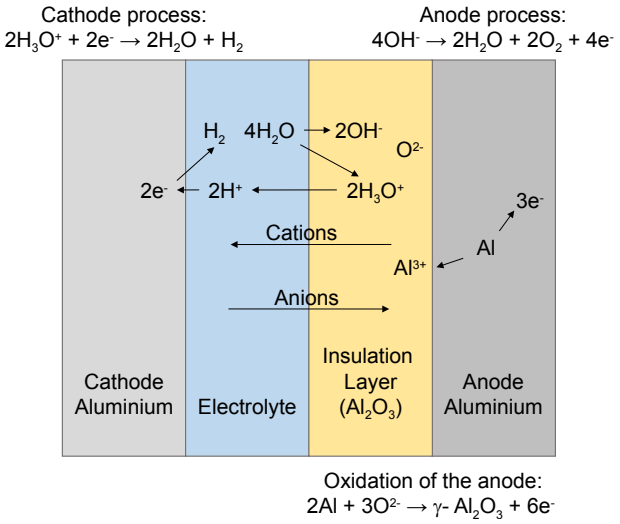


Fig. 1: Oxide-layer forming mechanism in an aluminium electrolytic capacitor.

The R_{ESR} is a construction dependent parameter, which contains the inner resistance of the conductive components (dielectric losses and ohmic resistance of raw materials, electrolyte, terminals and connections). This is a relatively small resistance but still not negligible. Beside the ripple current, these resistances are responsible for the temperature increase in the core. Reliability and lifetime of the capacitor are mainly influenced by the ripple current [22], [23] and [24].

There are numerous standards, which include the test procedures of aluminium electrolytic capacitors like: AEC-Q200, IEC 60384-1, IEC 60384-4 and CECC [14], [15] and [16]. Capacitor tests performed by manufacturers use mostly sinusoidal and constant voltage. Recently, PWM converters are widespread [1], [2], [3], [4], [5], [6], [8], [9], [10], [11], [12], [13] and [17]. Since these circuits operate switch-mode, the electrolytic capacitors are loaded with PWM voltage. Therefore, the load current of the capacitors is high-frequency rippled current, which causes substantial degradation in capacitor structural materials. The ESR value of PWM-loaded capacitor increases while the capacitance and weight decrease. The reduced capacitance and lower leakage current level imply the change of anode foil oxide layer. The standardized test procedures are not suitable for degradation analysis of capacitors loaded by square-wave current.

The calculation of core temperature can be scaled by correction factors to be valid for different ripple current waveforms [18] and [19]. Lifecycle calculations consider modified core temperatures by scaling factors for different ripple current waveforms. However, it is not revealed how life cycle varies at the same core temperatures when the capacitor is loaded by different ripple current. In this study, we analysed capacitor degradation caused by different ripple current waveforms at the same core temperatures.

2. Measurement Environment

For comparative analysis, different capacitors have been loaded by the standard sinusoidal current and PWM load.

During Endurance test with sinusoidal current, the capacitor current is sinusoidal. The ambient temperature is the recommended maximum operating temperature of the tested capacitor, usually 85 or 105 °C depending on its construction. The applied voltage is constant during the entire test duration and both the voltage and temperature are the rated values.

None of the standardized test procedures use high-frequency square-wave voltage to load the capacitor, therefore, a switch-mode power converter has been developed to ensure the PWM load to the analysed capacitor.

For degradation tests under PWM operation, a Two-Quadrant Chopper has been used, which contains the examined capacitor as can be seen in Fig. 2. The rated voltage of the capacitor meets the supply voltage of the converter. The converter contains an inductor (L) as output, which loads the capacitor (C). Two switches ensure the PWM voltage operation of the circuit.

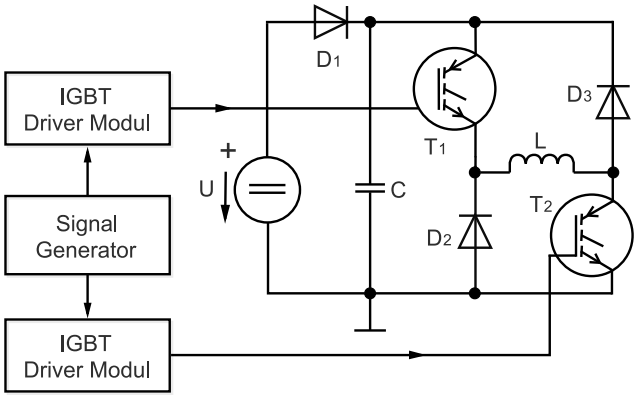


Fig. 2: The concept of the test bench.

The elements of the test circuit had to be appropriately chosen for the proper measurements. The initial parameters were the following: $C_R = 4700$ µF, $U_R = 400$ V, $ESR = 23$ mΩ, $Z = 28$ mΩ, $d = 76.9$ mm, $l = 105.7$ mm; $I_{AC,R} = 13.8$ A. The specifications of the circuit were the following: $f_s = 10$ kHz, $T = 10$ µs; the operating current and ripple: $I_{op} = 27.3$ A, $\Delta I_{op} = 2.7$ A, and the operating current of the capacitor was calculated from $I_{AC,R}$ at $U_T = 400$ V.

Tab. 1: Operating Leakage Currents (OLC) of the capacitors.

	OLC before tests (μA, measured after 24 h)		OLC after tests (μA, measured after 24 h)	
	Sinusoidal (50 Hz)	PWM (10 kHz)	Sinusoidal (50 Hz)	PWM (10 kHz)
Lot A	77.5	78.65	50.75	47.7
Lot B	109.3	114.11	62.6	50.4
Lot C	69.64	72.54	45.4	42.07
Lot D	101.75	106.37	68.17	48.78

The signal generator is based on SG3524 IC, which can generate accurate square waveform with variable duty cycle. The IGBT modules (SEMIKRON SKM 195GB126D) were driven by HCPL-3120 IGBT gate drive optocoupler circuits, which provides $+15/-5$ V signals. In order to minimize the losses, the inductor resistance (R_L) must be as small as possible, hence the value $R_L = 1\ \Omega$ has been chosen. It can be seen that in contrast to low resistance, relatively high power dissipation occurs.

The specified ripple current can be ensured by calculating the duty cycle (Eq. (2)) and the inductivity of the coil (Eq. (3)) as the following:

$$T_C = \frac{T}{2}\left(\frac{U_{avg}}{U} + 1\right) = 0.534 \cdot 10^{-4}\ \text{s}, \tag{2}$$

$$L \geq \frac{R}{f_s}\left(2\ln\frac{2U + R\Delta I_{op}}{2U - R\Delta I_{op}} + 1\right)^{-1} = 7.272\ \text{mH}. \tag{3}$$

The environment was verified based on SPICE circuit simulation of the model and the realized equipment was validated by test measurement. The circuit can generate the needed current stress for capacitor testing.

3. Test and Measurement Results

The 48 capacitors have been chosen from the rated voltage and capacitance domain of 400 V and 560 μF, respectively. The tested capacitors were grouped into four sets (Lot A – Lot D) based on their part numbers. Each group contains 12 capacitors, 6 for standard test, and 6 for PWM load test. The operating leakage current (I_{OLC}) was measured before the test procedure in order to verify the same initial conditions for all the tested capacitor pairs. The measurement was performed on 105 °C (the maximum operating ambient temperature of the capacitors) in a heating chamber. As can be seen in Tab. 1, the currents converge to the same values. Consequently, the conditions of the oxide layers were similar.

The capacitors were tested with both the standard equipment to perform sinusoidal tests and the developed test bench to perform PWM tests. The allowed maximum ratings (current and voltage level) for the alternating current tests were calculated according to the catalogue data of capacitors.

When capacitors were tested with PWM load, it was necessary to obtain the needed load current by Eq. (4), which is equivalent to the current applied in standard test. Capacitor ESR and power (P) are known as a result of standard procedures:

$$P = I^2 ESR(f). \tag{4}$$

The determined core temperature for all the tests was 109 °C in order to ensure identical test conditions for all capacitors and to avoid different capacitor degradation and electrolyte vaporization caused by different core temperatures. During test procedures, the core temperatures of the capacitors were measured with a K type thermocouple, which was inserted into the capacitor. Based on the measured core temperature, the duty cycle of the PWM voltage signal was adjusted to maintain 109 °C.

The weight and electrical parameters of the capacitors (C, ESR, Z) were measured at the beginning of the test and in every 250 hours.

Table 2, Tab. 3 and Tab. 4 show the aging effects of 50 Hz sine and 10 kHz PWM voltage signals on the capacitors at 20 °C ambient temperature.

The 10 kHz PWM voltage signal test resulted in more intensive aging than the standard sinusoidal endurance test: higher rate of capacitance reduction, weight loss and ESR increase were noticed. The weight loss indicates the evaporation of the electrolyte, while the change of the capacitance and ESR identify the structural, chemical and volumetric transformation of the anode, cathode and the electrolyte. The capacitance values decrease that can be explained by the reduction of conducting plates (the charge storing capacity of anode foil is less) and/or distance increase between them.

After the alternating current tests, the OLC measurements were performed. The values of steady-state OLCs were categorized in Tab. 1 for all tested capacitors. The OLC measurements of Lot B can be seen in

Tab. 2: Capacitance change of the capacitors.

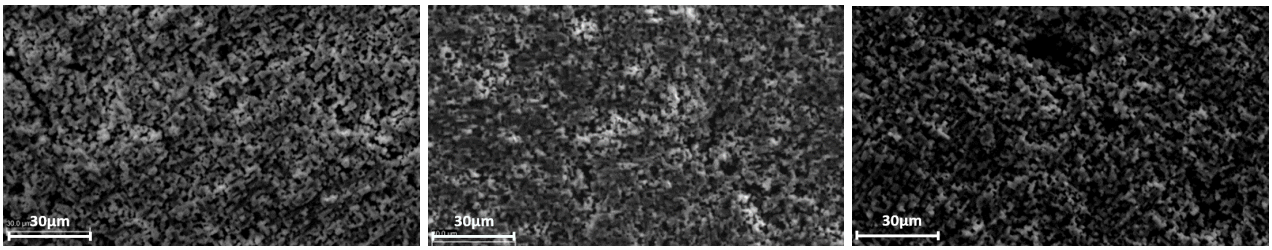
Measurement time (h)	Capacitance change (%, measured at 120 Hz, 20 °C)							
	Lot A		Lot B		Lot C		Lot D	
	Sinusoidal (50 Hz)	PWM (10 kHz)	Sinusoidal (50 Hz)	PWM (10 kHz)	Sinusoidal (50 Hz)	PWM (10 kHz)	Sinusoidal (50 Hz)	PWM (10 kHz)
0	0	0	0	0	0	0	0	0
250	−1.03	−1.32	−1.3	−1.8	−0.88	−0.81	−0.31	−1.13
500	−1.05	−1.48	−2.56	−3.54	−2.09	−2.42	−1.23	−2.21
750	−1.5	−1.64	−4.06	−4.25	−3.18	−3.63	−2.51	−3.2

Tab. 3: ESR change of the capacitors.

Measurement time (h)	ESR change (mΩ, measured at 120 Hz, 20 °C)							
	Lot A		Lot B		Lot C		Lot D	
	Sinusoidal (50 Hz)	PWM (10 kHz)	Sinusoidal (50 Hz)	PWM (10 kHz)	Sinusoidal (50 Hz)	PWM (10 kHz)	Sinusoidal (50 Hz)	PWM (10 kHz)
0	104.77	104.91	112.56	113.29	104.74	102.95	93.44	92.42
250	106.9	107.38	119	123	116.42	116.62	101.68	100.59
500	111.18	112.62	138.2	148.07	142.8	144.57	107.8	108.89
750	115.34	117.64	153.75	166.29	162.38	165	113	114.93

Tab. 4: Weight loss of the capacitors.

Measurement time (h)	Weight loss (g)							
	Lot A		Lot B		Lot C		Lot D	
	Sinusoidal (50 Hz)	PWM (10 kHz)	Sinusoidal (50 Hz)	PWM (10 kHz)	Sinusoidal (50 Hz)	PWM (10 kHz)	Sinusoidal (50 Hz)	PWM (10 kHz)
0	0	0	0	0	0	0	0	0
250	0.02	0.04	0.12	0.16	0.05	0.09	0.12	0.08
500	0.04	0.11	0.19	0.21	0.11	0.19	0.15	0.19
750	0.09	0.14	0.23	0.27	0.17	0.28	0.27	0.32



(a) 10 kHz alternating current test. (b) Standard test. (c) Reference.

Fig. 3: Electron microscopy captures snapshot of anode foil.

Fig. 4 in detail. Both the waveforms and the steady-state values of OLCs are different after performing AC voltage tests. During 50 Hz and 10 kHz tests, the structure of the oxide layer was erratically transformed. The spikes in the current waveforms can be explained by the deformed spatial structure of the oxide layer. When analysing the current waveform after 10 kHz test, it can be concluded that spikes are more relevant. Lower leakage current level can be observed in steady-state because of the thickened oxide layer of anode. Since the oxide layer went through a more significant deformation, the OLC has less steady-state value when the capacitor was tested with 10 kHz PWM signal instead of 50 Hz sine wave.

Both the capacitance and OLC reduction imply anode foil structural change. Therefore, the anode foils were investigated with structural analysis. The morphology of the anode foil surface was investigated with a scanning electron microscope. As can be seen in Fig. 3, there are no significant differences between the results, hence the pore size distribution was examined in order to find the reason for the capacitance and OLC reduction.

The results were obtained from the pore size distribution and the specific surface area examinations. Micro- and macroporosity, as well as specific surface area, were measured by mercury intrusion and nitrogen adsorption porosimeters, after eight hours vacuum treatment on 125 °C.

The change of the specific surface area was determined by nitrogen adsorption and the pore size distribution was used for characterization of the degrada-

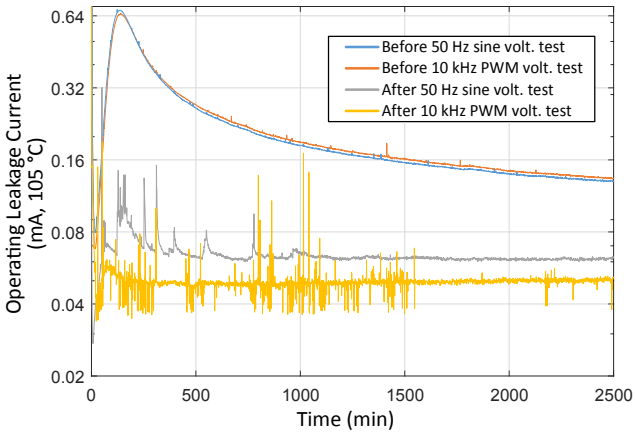


Fig. 4: Operating leakage currents of Lot B capacitors.

tion of the anode surface. The differential logarithmic pore volume functions in the range of 10–10000 nm have a maximum in the interval of 1000–2000 nm pore diameters. This maximal (Fig. 5) value is shifted to a smaller (600–700 nm) pore size in the case of the capacitor tested on 10 kHz PWM voltage signal. It means that the pits diameter of the foil narrowed during the high-frequency test.

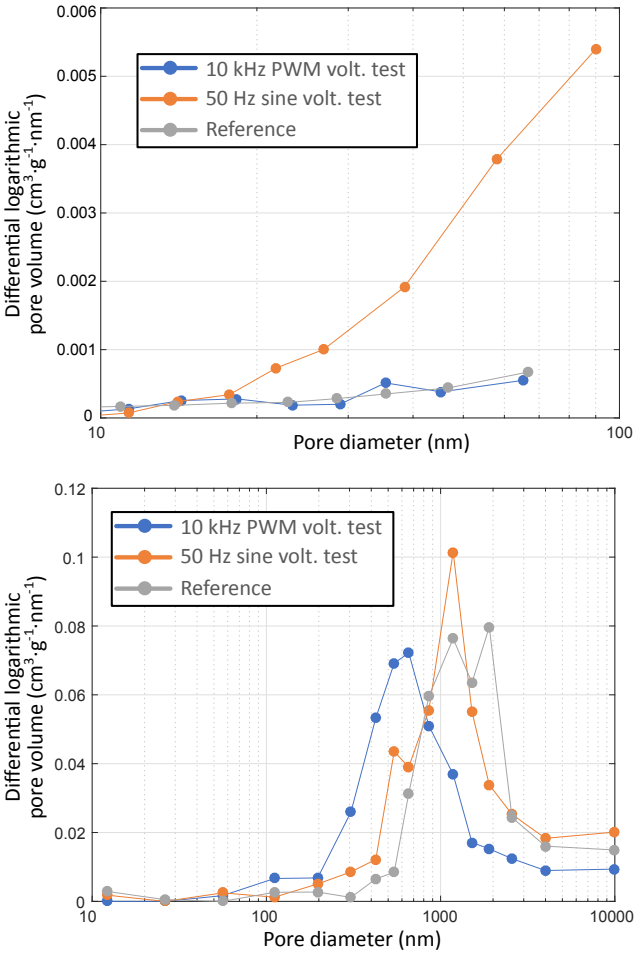


Fig. 5: Pore volume distribution.

4. Conclusions

The general problem with the electrolytic capacitor is the electrolyte vaporization during operation. Core temperature is an important property of the tests because it influences the level of the degradation. It is also affected by ambient temperature and load current. The capacitors are loaded by dynamically changing current in modern switched power electronics applications. The standard validation test methods work with sinusoidal load current only. During tests, square-wave voltage was applied (10 kHz PWM) on the tested capacitor beside the standard sinusoidal voltage (50 Hz). The general electrical parameters of capacitor were analysed. These values show that the PWM current cause more severe degradation than sinusoidal load current. The ESR values are increased, while the capacitance and weight decreased more than in the case of the standard sinusoidal endurance test. The reduced capacitance and lower leakage current level imply the change of anode foil oxide layer.

In order to analyse the structural change of the anode material, micro- and macroporosity, as well as specific surface area, were measured by mercury porosimeter. The pore size distribution showed that the PWM voltage based current load decreased the pore diameter of the capacitor anode foil. It initiated an oxide layer formation, which consumes the electrolyte. Therefore, the electrolyte transformation is accelerated which leads to faster aging and shorten the lifetime.

The analyses showed that the introduction of a new type of standard test, namely testing the degradation under PWM load is worth to estimate the life span of capacitors in PWM power converters.

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