Novel Ternary Logic Gates Design in Nanoelectronics

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DOI: 10.15598/aeee.v17i3.3156

Abstract. *In this paper, standard ternary logic gates are initially designed to considerably reduce static power consumption. This study proposes novel ternary gates based on two supply voltages in which the direct current is eliminated and the leakage current is reduced considerably. In addition, ST-OR and ST-AND are generated directly instead of ST-NAND and ST-NOR. The proposed gates have a high noise margin near $V_{DD}/4$. The simulation results indicated that the power consumption and PDP underwent a sharp decrease and noise margin showed a considerable increase in comparison to both one supply and two supply based designs in previous works. PDP is improved in the proposed OR, as compared to one supply and two supply based previous works about 83 % and 63 %, respectively. Also, a memory cell is designed using the proposed STI logic gate, which has a considerably lower static power to store logic '1' and the static noise margin, as compared to other designs.*

Keywords

CNTFETs, double supply voltages, static power reduction, ternary logic gates, ternary memory cell.

1. Introduction

Typically, digital circuits with two logic levels are designed in the binary space; however, binary logic can be employed in designing digital circuits by adding several other logic levels called Multiple-Valued Logic (MVL) [1]. Compared to the binary logic, the ternary logic can transmit further information from a set of lines with less memory and easier access and lower power consumption by reducing the chip level and decreasing the internal and external connections. In addition, parallel serial operations can be performed more quickly. One of the main drawbacks of multi-valued logic is the lower Noise margin, as compared to the binary logic [2], [3], [32], [33] and [34].

The implementation of the CMOS circuits has reached a limitation [4]. CNTFET is another candidate which does not have leakage current, such as MOSFET, but it suffers from a disturbing current of Band-To-Band Tunnelling (BTBT) [5]. The Carbon Nanotube Field-Effect Transistor (CNTFET) is a good alternative to the CMOS transistors for the implementation of logic circuits due to its high performance and low power consumption [6], [7], [8], [9] and [10]. Also, carbon nanotube transistors can be a good option for designing ternary circuits with less complexity due to their good ability to change the threshold voltage, which is caused by a change in the diameter of nanotubes [11].

Several researches have been done in recent years on the design of ternary and quaternary circuits with the help of carbon nanotubes transistors, such as [14], [28] and [31]. Some studies have been conducted on the design of ternary gates based on CNTFETs [11], [12], [13], and [29]. The design of Lin et al. [13] can be mentioned as the best one based on one supply voltage, in which, for generating logic '1' in the output (STI, ST-NAND, ST-NOR), a voltage divider circuit is used, with the diode connection load to reduce the direct current.

In some studies like [22] and [23], two supply voltages are used in the ternary circuit design for simplicity, but the direct current hasn't been removed

Tab. 1: Ternary NANDs and NORs truth table.

A	B	ST-NOR	PT-NOR	NT-NOR	ST-NAND	PT-NAND	NT-NAND
0	0	2	2	2	2	2	2
0	1	1	2	0	2	2	2
0	2	0	0	0	2	2	2
1	0	1	2	0	2	2	2
1	1	1	2	0	1	2	0
1	2	0	0	0	1	2	0
2	0	0	0	0	2	2	2
2	1	0	0	0	1	2	0
2	2	0	0	0	0	0	0

and the static power dissipation still exists. In [29], ternary gates are designed based on two supply voltages. In [14], two supply voltages are used in a multiplexer scheme to ternary multiplier, reporting a considerable static power reduction. In [26], ternary logics like full adders are synthesised using the 2:1 multiplexer, in which logic '1' is directly switched to the output and a considerable reduction in power and PDP is obtained. In [29], ternary gates are designed based on two supply voltages. In this paper, V_{DD} and $V_{DD}/2$ voltage sources are used to design new ternary logic gates as the standard ternary inverter, the ternary buffer, standard ternary OR (ST-OR) and standard ternary AND (ST-AND). To generate logic '1', $V_{DD}/2$ source is directly switched to the output with a novel structure and all direct paths from V_{DD} to the ground are removed in the circuit design, which sharply decreases static power consumption. Also, cascode NTI and PTI, according to the [29], are used to reduce the leakage current. However, the drawback of using two supply voltages is that excess lines are needed for $V_{DD}/2$; despite this, if the design is done so as to remove all direct paths from the sources to ground, they can be sharply decreased in static power dissipation and PDP is more important than the excess line in some applications. For example, in the memory cell, the circuit may stay in one status for a relatively long time; so, the dynamic power in transistors and connections is little in contrast to the static power dissipation from the voltage division to produce logic '1'. However, it is a trade-off between a higher power and the excess lines for $V_{DD}/2$. So, Designers can use two supply-based ternary circuits for some low static power designs and for other portions of logic systems, one supply voltage gates with high static power dissipation and lower metal connections can be used.

Simulation results using the HSPICE software and the CNT 32 nm Stanford library [16] indicated the lower power dissipation and PDP, as compared to the previous designs. Also, the proposed Standard Ternary Inverter (STI) is used to design the new ternary memory cell, where the stored static power is sharply reduced, as compared to other designs.

2. Terminology

The chiral vector for a CNT is represented by a pair of integers (m, n) [15] and [27]. The dimensions of the nanotube can be defined by the relation

$$D_{CNT} = \frac{a_0\sqrt{3}}{\pi}\sqrt{n^2 + m^2 + nm}, \tag{1}$$

where $a_0 = 0.142$ nm is the atomic distance between each carbon atom and its adjacent atom [16], [17] and [18]. The value of the threshold voltage of the carbon nanotubes transistor is determined by the relation

$$V_{th} \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{CNT}}, \tag{2}$$

where $a = 2.49$ A, $V_\pi = 3.033$ eV, and e is the unit electron charge.

For chirality (0, 19) and (0, 10), the diameter of the nanotubes will be 1.487 nm and 0.787 nm, respectively, [16], [17] and [18]. It is possible to add up the relationship between the threshold voltage and the nanotubes' diameters as $V_{th} = \frac{0.35}{D_{CNT}}$ [19] and [28].

Ternary circuits including inverters are NAND and NOR gates, by which most of the designs are conducted. The Ternary logic operation can be defined as follows, where $X_i, X_j = \{0, 1, 2\}$ [20].

$$\begin{aligned} X_i + X_j &= \max\{X_i, X_j\}, \\ X_i \cdot X_j &= \min\{X_i, X_j\}, \\ \bar{X}_i &= 2 - X_i. \end{aligned} \tag{3}$$

As such, $(-)$ denotes subtraction and $(+)$, $(.)$, and $(+)$ operators refer to standard ternary OR (ST-OR), standard ternary AND (ST-AND), and Standard Ternary Inverter (STI), respectively, in the Ternary logic whose circuit structure will be further described. NAND and NOR ternary gates are operators with double entries. These gates are defined using Eq. (4) and Eq. (5) [3].

$$Y_{\text{NAND}} = \overline{\min\{X_i, X_j\}}, \tag{4}$$

$$Y_{\text{NOR}} = \overline{\max\{X_i, X_j\}}. \tag{5}$$

Table 1 shows the truth table for the NAND and NOR gates in the Negative (NT), Positive Ternary (PT) and Standard Ternary (ST) modes. The difference between the outputs of these modes with those in the standard mode is in the logic '1' output. When the output becomes '1' in ST-NAND and ST-NOR modes, in PT-NAND and PT-NOR modes, the output becomes '2', while in the NT-NAND and NT-NOR mode, it becomes '0', respectively [3]. Also, Positive Ternary Inverter (PTI) and negative ternary inverter are two types of ternary inverter, in which, when the output of STI is '1' for PTI and NTI are '2' and '0' respectively.

3. Proposed Ternary Logic Gates

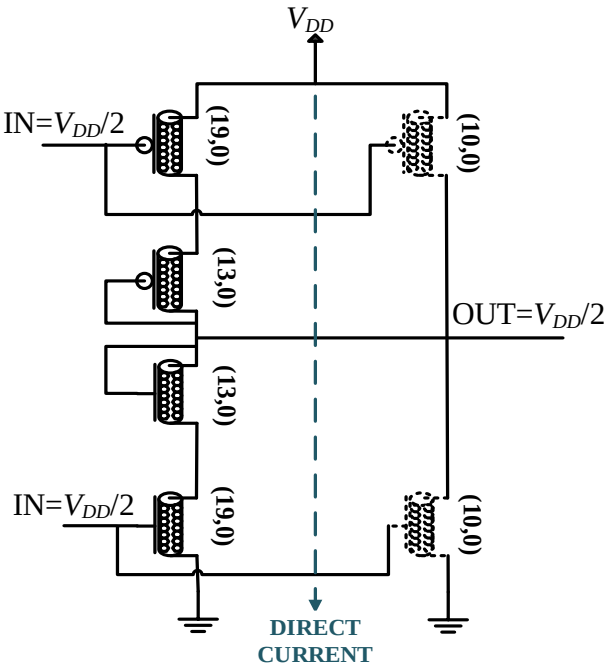


Fig. 1: STI designed in [13].

In the one supply based ternary logic gates for metal connections reduction, a V_{DD} voltage source was assumed. In the standard mode, pull up and pull down networks are simultaneously turned on as a voltage divider for generating logic '1', which leads to a high static power to produce logic '1' for example, Fig. 1 displays the STI circuit designed in [13] when the input is logic '1'. The transistors which are off are dimmed in the figure. As can be seen, T2, T3, T4, T5 are simultaneously turned on, acting as a voltage divider to produce $V_{DD}/2$ at the output. This leads to a direct current from V_{DD} to ground. One superiority of this design, as compared to the previous work, is using the diode-connected transistors T3 and T4 to reduce the direct current, but static power is much higher than the dynamic power of CNTFETs; this will be discussed in the simulation results section.

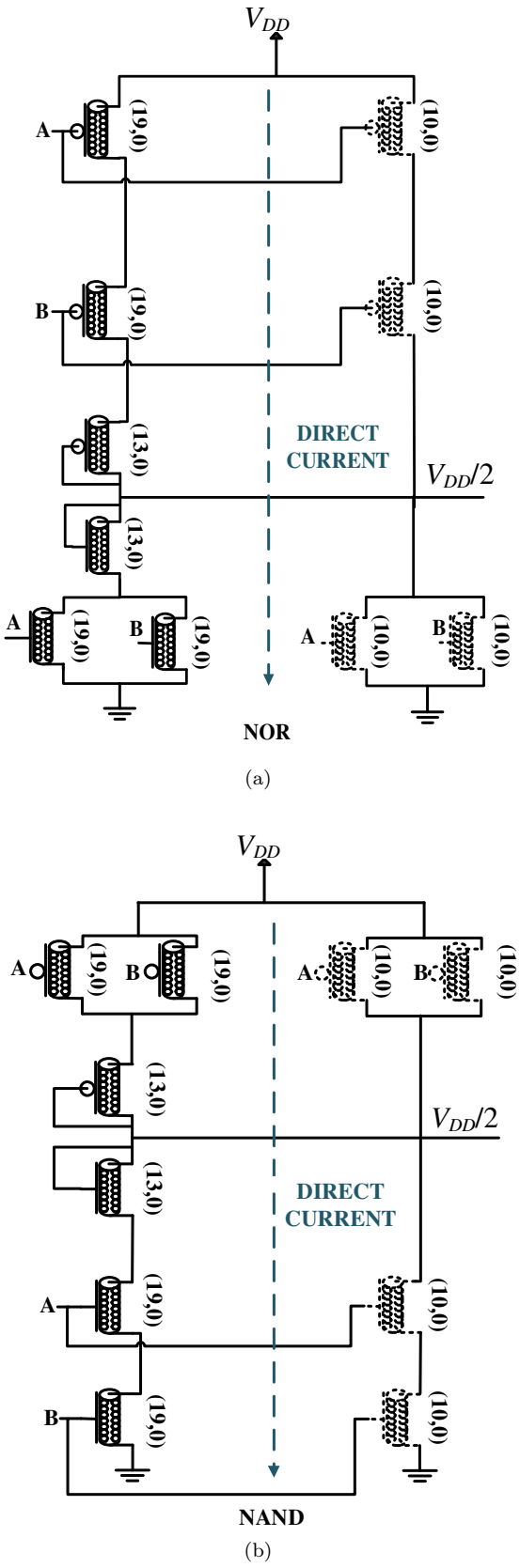


Fig. 2: (a) ST-NOR and (b) ST-NAND designed in [13].

Also, the same manner is used to design ST-NAND and ST-NOR; a direct path is connected from V_{DD} to the earth, generating static power when the output is $V_{DD}/2$. In Fig. 2, the transistors which are off are dimmed [13].

3.1. The Proposed Ternary BUFFER and STI

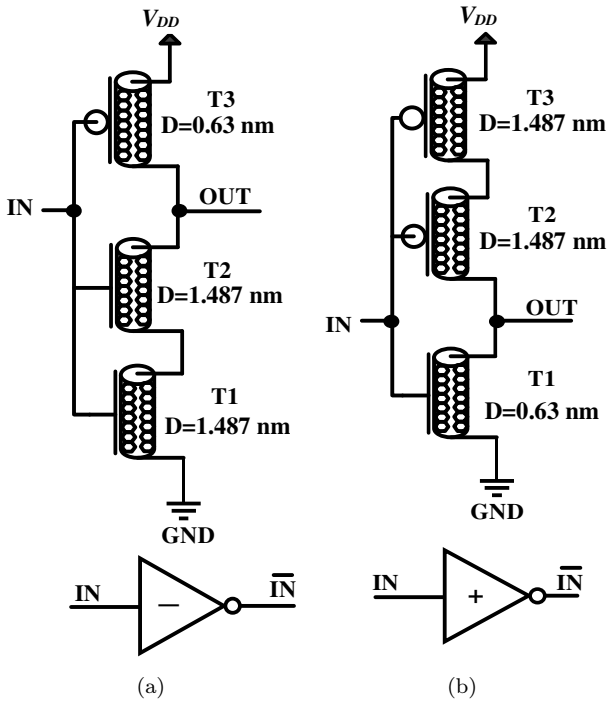


Fig. 3: (a) Cascode - NTI and (b) Cascode - PTI [30].

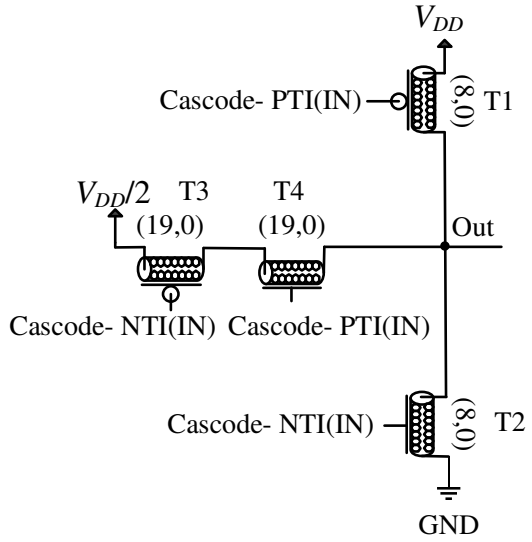


Fig. 4: Proposed buffer.

The proposed buffer and STI circuit are shown in Fig. 4 and Fig. 5, respectively. As can be seen in Fig. 3, based on the status of input, the off state transistors are shown as dotted. The situation of transistors in different statuses is as follows:

In case the input equals '0', both PTI and NTI outputs are '2'.

In case input equals '2', both PTI and NTI outputs are '0'. The output is connected to the Ground by T1 in STI, and V_{DD} via T2 in the buffer.

In case the input equals '1', the PTI output is '2' and the NTI output is '0', and the $V_{DD}/2$ supply voltage is switched to the output by T3 and T4 for both STI and buffer.

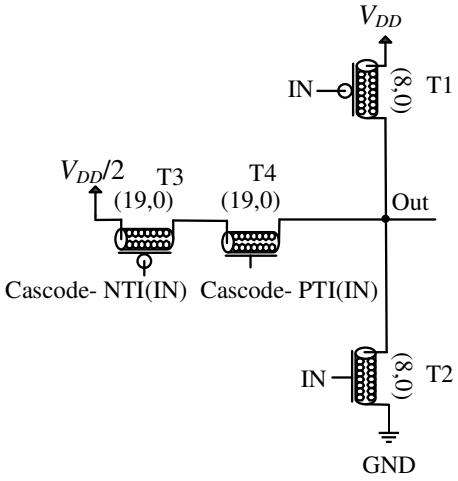


Fig. 5: Proposed STI.

As can be seen in all three cases, there is no direct path from V_{DD} to Ground, and the static power consumption is minimized considerably in the proposed circuit. Also, to reduce the leakage current in NTI and PTI according to the [30], the cascade NTI and PTI are used.

3.2. Proposed Standard Ternary AND (ST-AND)

The ST-AND circuit is designed according to Fig. 6. In this figure, the nodes of X and Y are connected to the outputs of PT-NAND and NT-NAND, respectively. According to Fig. 7, based on the inputs statuses, the off state transistors are depicted as dotted.

As stated in Tab. 1, PT-NAND and NT-NAND have the same output as ST-NAND; only in case the ST-NAND output is equal to '1', the PT-NAND output equals '2' and NT-NAND is equal to logic '0'.

The circuit description is as follows:

According to Tab. 1, the ST-AND output must be '2' when the PT-NAND and NT-NAND outputs are '0'. In this case, T2 and T4 are turned on and T1 and T3, are off, and the output is connected to V_{DD}.

According to Tab. 1, it is expected that the output of the ST-AND would be '0', where PT-NAND and NT-NAND equal '2'. In this case, the transistors T1 and T3 are on and the transistors T2, T4 are off. The output is connected to the earth.

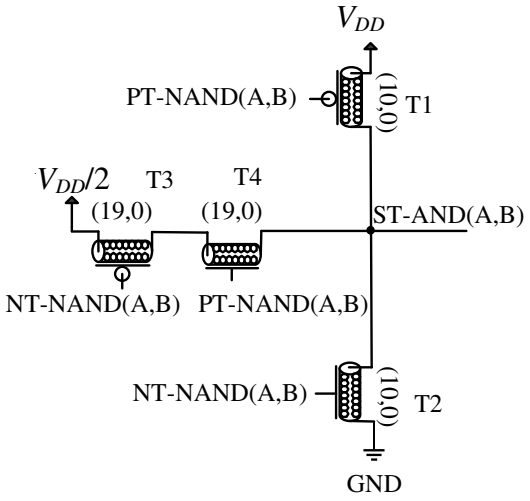


Fig. 6: ST-AND proposed circuit assuming.

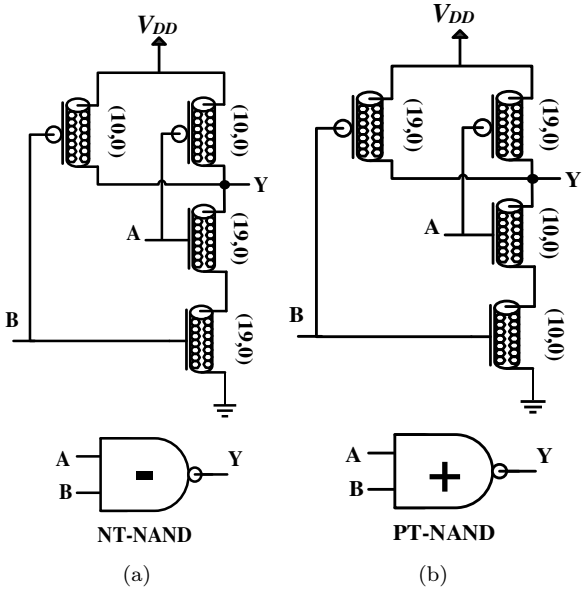


Fig. 7: (a) NT-NAND and (b) PT-NAND circuits.

It is expected that the ST-AND and ST-NAND outputs would be equal to '1', where PT-NAND is equal to logic '2' and NT-NAND is equal to logic '0'. In this case, transistors T1 and T2 are off and the transistors T3, T4, are on; further, the output is connected to the $V_{DD}/2$ supply voltage. As can be seen, V_{DD} is not connected to the Ground in any case. Also, PT-NAND and NT-NAND have no direct paths from V_{DD} to the Ground.

3.3. Proposed Standard Ternary OR (ST-OR)

Figure 8 indicates the proposed ST-OR circuit, where the nodes X and Y are the outputs of PT-NOR and NT-NOR, respectively, according to Fig. 9. As shown in Tab. 1, the NT-NOR and PT-NOR outputs are the same outputs as ST-NOR, except logic '1', where the NT-NOR output equals the logic '0', and the PT-NOR equals the logic '2'. The circuit demonstration is the same as ST-AND; so, it is not repeated here.

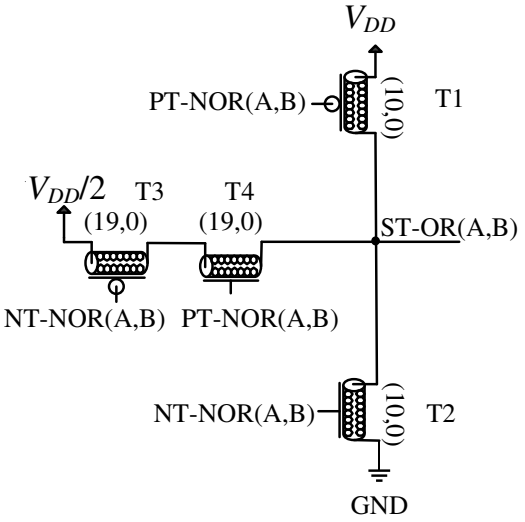


Fig. 8: Proposed ST-OR circuit assuming.

In the studies [12], [13] and [14], STI, ST-AND, ST-OR are used to design the ternary half adder, the full adder and the multiplier. In the [24], these gates are used to design the ternary subtract or the comparator, the full adder, and the multiplier. In [21], STIs are used to design the first ternary, as compared to a study conducted in [13]; in the proposed designs, the power consumption has fallen by about 17 times; however, the delay in the proposed method is slightly higher. Eventually, PDP as the main criterion is decreased by about 10 times. The power reported for the proposed design is the total power dissipated from both voltage sources, as NAND and NOR have been designed in the previous memory cell. In this paper, given the importance of static power in the memory cell, the proposed STI is used to design a memory cell.

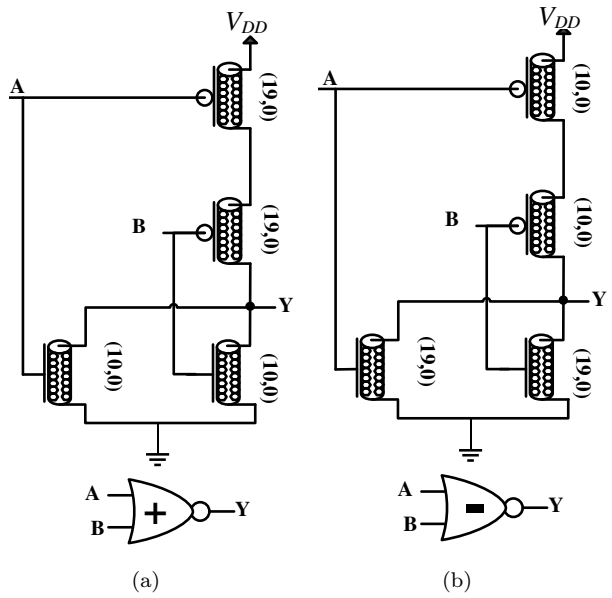


Fig. 9: (a) PT-NOR b) NT-NOR circuit.

3.4. Proposed Memory Cell

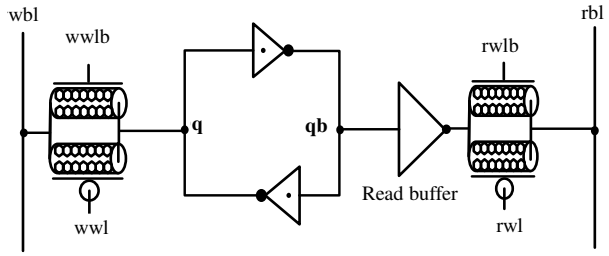


Fig. 10: Proposed CNTFET-based ternary memory cell based on [21].

As mentioned before, in the memory cell, the circuit may stay in one status for a relatively long time; so, according to the low frequency, the dynamic power in transistors and connections is negligible in contrast to the static power dissipation from the voltage division to produce the logic '1'. The designed memory cell is based on the ternary memory cell design in [21], where the proposed STI is replaced in the latch and read buffer, shown in Fig. 10. As the binary latch consists of two cross-coupled inverters, the cross-coupled STIs can be locked in three states (q, qb) = ('0', '2'), ('2', '0') and ('1', '1'). The STIs in [13] are used for the designed ternary memory cell in [21], as shown in Fig. 1. Also, in the memory cell designed in [25], the same STIs are used. In these memory cells, when the latch is locked in the ('1', '1') state, the direct current flows from V_{DD} to the ground for both STIs. So for storing '1' in these memory cells, a high power would be dissipated, as compared to other states ('0' and '2'). But, by using the proposed STI, the same static power is expected for three states of storing.

4. Simulation Results

The simulation results of the proposed circuit are utilized using the HSPICE Synopsys software and the 32 nm model of Stanford University [16]. The voltages required for this circuit are 0.9 V and 0.45 V, respectively. The logic gates designed with the previous works were evaluated based on various parameters discussed accordingly. Table 2 shows the power, delay, and Power Delay Product (PDP) of different designs.

Tab. 2: Comparison of ternary logic gates.

STI [13]	2.5	0.269	0.672
NOR+STI OR [13]	6	0.7391	5.9128
NOR [13]	3	0.4676	1.4028
NAND +STI [13]	7.2	0.7349	7.4959
NAND [13]	3	0.4629	1.3889
STI [29]	5.08	0.06	0.304
STNOR [29]	16	0.04	0.64
STNAND [29]	12	0.04	0.48
NOR+STI OR [29]	22.02	0.09	1.981
NAND+STI (AND) [29]	17.1	0.09	1.539
Proposed STI	4.2	0.0089	0.0373
Proposed buffer	8.5	0.0079	0.067
Proposed OR	8	0.02897	0.2312
Proposed AND	12	0.03521	0.4224

As shown in Tab. 2, PDP is improved in the proposed OR, as compared to NOR [13] (one supply) and NOR [29] (two supply), which were about 83 % and 63 %, respectively. If the proposed OR is compared by NOR + STI (to produce OR) for [13] and [29], the PDP is decreased by about 96 % and 85 %, respectively. Also, PDP is improved in the proposed AND, as compared to NAND [13] (one supply) and NAND [29] (two supply), which were about 69 % and 12 %, respectively. If the proposed OR is compared by NAND + STI (to produce AND) for [13] and [29], the PDP is decreased by about 94 % and 72 %, respectively. In the case of the proposed ternary buffer, the PDP improvement in the comparison with the case of combining two STIs to produce the buffer in [13] and [29], is about 95 % and 89 %, respectively.

Static power consumption is an important criterion in the design of digital circuits, since circuit may stay in a logic level for a long time (like memory cell). The static and dynamic power for STI in different modes is plotted in Tab. 3. The static power for the proposed design is reported as the total static power dissipated from both voltage sources (V_{DD} and $V_{DD}/2$). Also,

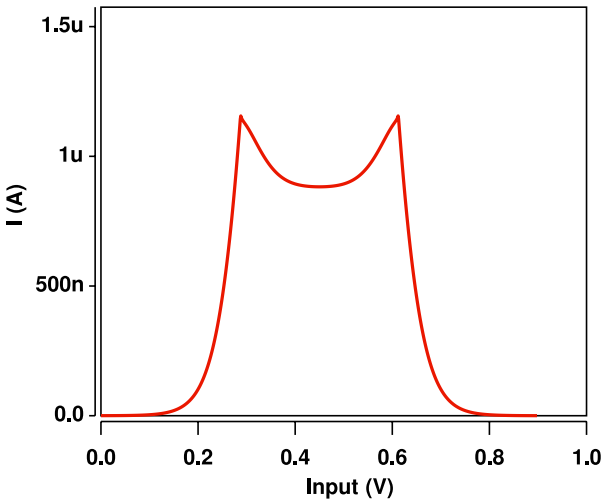
Fig. 11 shows the current drawn from the source for the proposed STI and [13].

Tab. 3: Static power table for proposed STI.

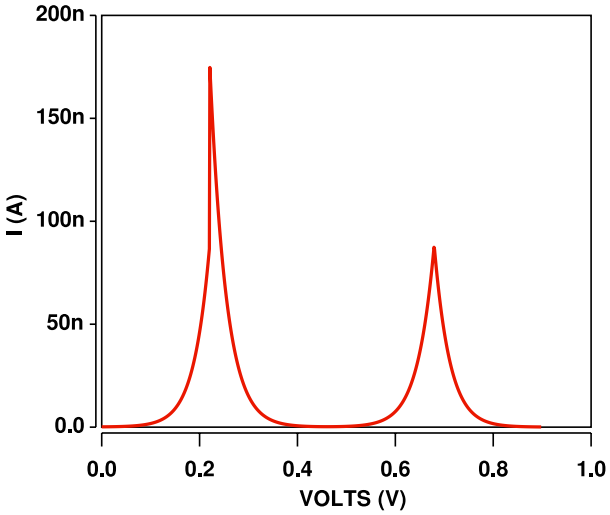
Input	STI Proposed (nW)	STI [13] (nW)	STI [29] (nW)
0 V	0.015	0.17	0.18
0.45 V	0.13	794.21	38.37
0.9 V	0.018	0.13	0.14

Tab. 4: Power consumption table for proposed STI.

Design	Static Power (nW)	Dynamic Power (nW)	Total Power(nW)
Proposed	12.89	27.91	40.72
[13]	264.83	61.61	326.41
[29]	14.53	280.00	51.22

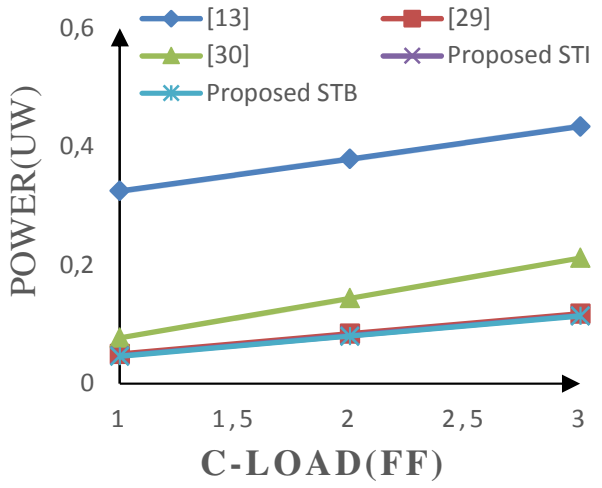


(a) [13].

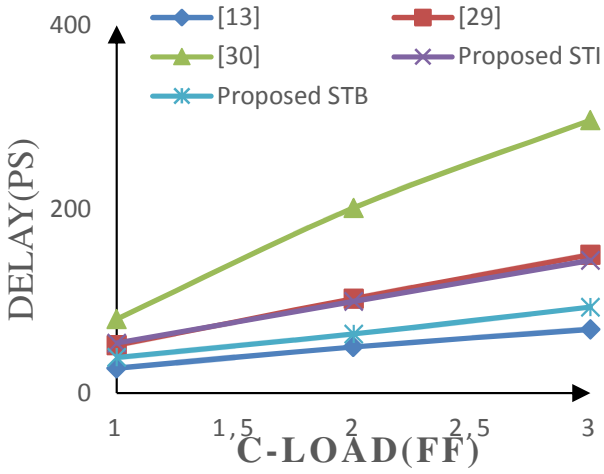


(b) Proposed.

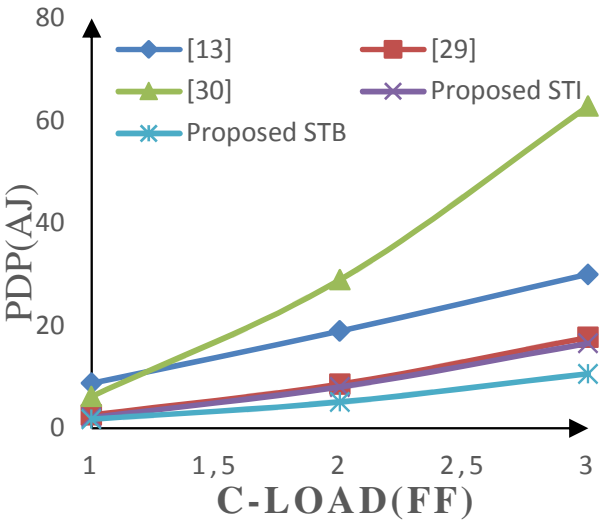
Fig. 11: Current drawn from the power supply against the input.



(a) Power.

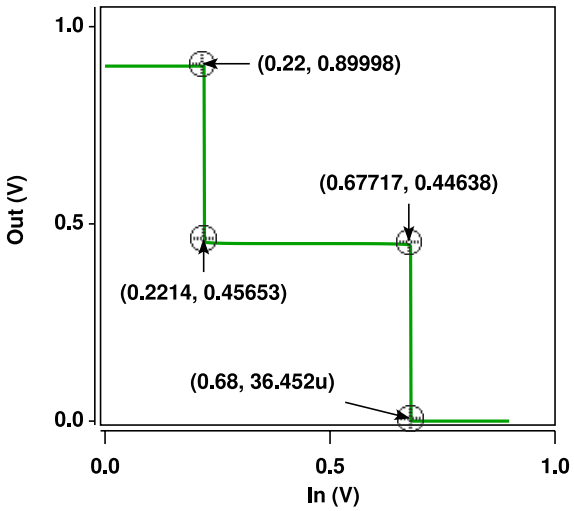


(b) Delay.

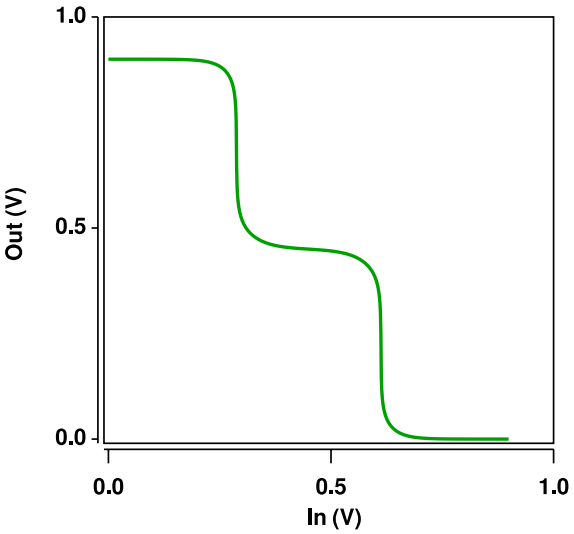


(c) PDP.

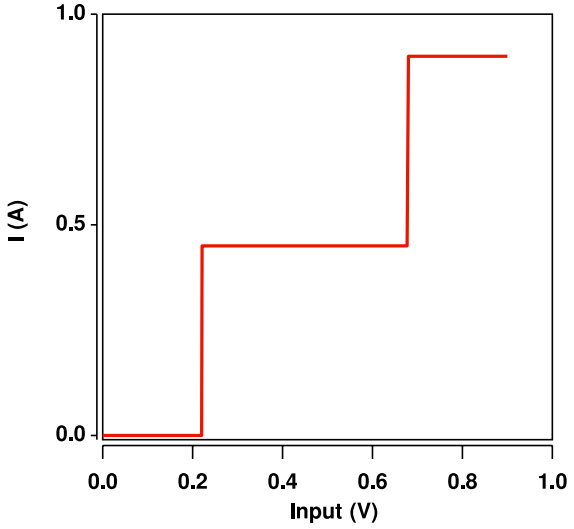
Fig. 12: Evaluation the STIs under different loads.



(a) Proposed STI.



(b) STI of [13].



(c) Proposed Buffer.

Fig. 13: Voltage Transfer Characteristic (VTC) of different designs.

As shown in Tab. 3, when the output is '1', high static power can be obtained by considering the direct current from V_{DD} to the ground [13]. However, in the proposed method and the recent study, the static power is minimized considering the current direct path removal. This is shown in Fig. 9, where the static power versus input voltage can be seen; as shown, the current and static power are greatly decreased in the logic '1' mode in the proposed method. Table 4 separately presents the dynamic power and static power for STIs. As can be seen, the proposed STI has a lower static power dissipation. Although the power dissipation is minimized using only one supply voltage in [30], by increasing the resistance in the voltage division path, the driving ability is reduced considerably.

As can be seen in Fig. 12, delay is considerably enhanced by increasing the load capacitance; so, PDP is increased considerably by increasing the load capacitance for the STI design of [30]. As can be seen, in this proposed STB, PDP is better in different loads.

The Transfer Characteristics (VTC) of the proposed STI and STI [13] are shown in Fig. 13. As can be seen, the transfer characteristic of the proposed circuit had a better noise margin due to sharper transient near $V_{DD}/4$ and $3V_{DD}/4$. To calculate the noise margin in accordance with the references [19] and [27], first, V_{i0}, $V_{i1}-$, $V_{i1}+$, V_{i2}, V_{O0}, $V_{O0}-$, $V_{O0}+$ and V_{O2} were obtained from the VTC curve, as shown in Fig. 13(a). Then, according to the following equations and comparison with Tab. 5, the noise margin is calculated.

$$\begin{aligned} NM_1^- &= V_{O1}^- - V_{I1}^-, \\ NM_0 &= V_{I0} - V_{O0}, \\ NM_1^+ &= V_{I1}^+ - V_{O1}^+, \\ NM_2 &= V_{O2} - V_{I2}. \end{aligned} \tag{6}$$

As can be observed, the proposed design had a considerably better noise margin in comparison to that in [13] and [29].

Tab. 5: Noise margin of the STI.

Design	NM "0" (mV)	NM "1⁻" (mV)	NM "1⁺" (mV)	NM "2" (mV)	NM (mV)
[13]	180	120	160	210	120
[29]	280	160	160	270	160
Proposed	219	224	224	219	219

Figure 14 shows the write operation for the proposed ternary memory cell. The simulation results of storage power dissipation are compared in Tab. 8, which consists of the static power dissipated from both supply voltages. As can be seen, the storage power in the proposed memory cell for storing the logic '1' is sharply reduced from $8.287 \cdot 10^{-7}$ W in the design [21], $4.48 \cdot 10^{-8}$ W in the design [25], and $9 \cdot 10^{-10}$ W in the

Tab. 6: Write delay of the ternary memory cell.

Design	Write 0 → 1	Write 1 → 2	Write 2 → 0	Write 0 → 2	Write 2 → 1	Write 1 → 0
[21]	24.45 ps	2.59 ps	10.90 ps	10.64 ps	24 ps	3.4 ps
[25]	21.12 ps	3.71 ps	15.66 ps	6.2 ps	21.34 ps	9.085 ps
[30]	8.3 ps	5 ps	9.3 ps	12 ps	11.03 ps	8 ps
Proposed	9 ps	4 ps	6 ps	10.5 ps	12.5 ps	2 ps

design [30] to $2.7 \cdot 10^{-10}$ W according to removing the direct current. The range of static power for storing '1' in the proposed memory cell is like storing '0' and '2'. The average delay in different states is reported in Tab. 8, which is almost in the same range in all designs in the [30]; by using high resistance, the direct current is reduced considerably against other designs, but the proposed design has 87 % less static power to store logic '1'. Table 6 and Tab. 7 show the read and write delay for different designs; as can be seen, the proposed design has lower read and write delay, unlike other designs.

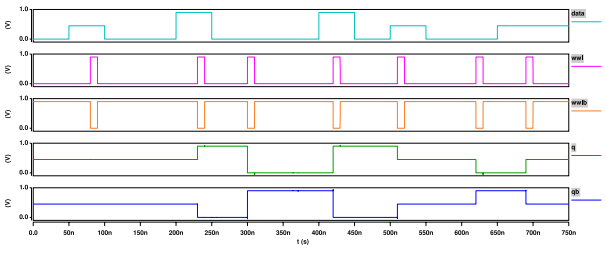


Fig. 14: Write operation of the proposed ternary memory cell.

Tab. 7: Read delay of the ternary memory cell.

Design	Read "0" (ps)	Read "1" (ps)	Read "2" (ps)
[21]	127	39	135
[25]	55.1	18.9	20.1
[30]	48.3	22.17	29.4
Proposed	36	15	25

Tab. 8: Standby power of the ternary memory cell.

	Strong "0" (W)	Strong "1" (W)	Strong "2" (W)
[21]	$3.515 \cdot 10^{-10}$	$8.287 \cdot 10^{-7}$	$5.104 \cdot 10^{-10}$
[25]	$3.21 \cdot 10^{-10}$	$4.48 \cdot 10^{-8}$	$1.52 \cdot 10^{-10}$
[30]	$7 \cdot 10^{-10}$	$9 \cdot 10^{-10}$	$7 \cdot 10^{-10}$
Proposed	$3.43 \cdot 10^{-11}$	$2.7 \cdot 10^{-10}$	$3.42 \cdot 10^{-11}$

Figure 15 shows the butterfly diagram of the latch proposed. To obtain the Static Noise Margin (SNM) of the proposed latch, the diameter of squarer surrounded by eyes was considered, as reported in Tab. 9. As can be seen, by the proper adjustment of nanotube diameters in the STI, a sharp transient in $V_{DD}/4$ and $3V_{DD}/4$ was achieved, causing a high SNM in the proposed memory cell and an almost equal value for storing all three states. Also, the design of [30] has a very good SNM. But other designs have considerably lower SNM for storing logic '1', leading to a considerable lower SNM for the latch.

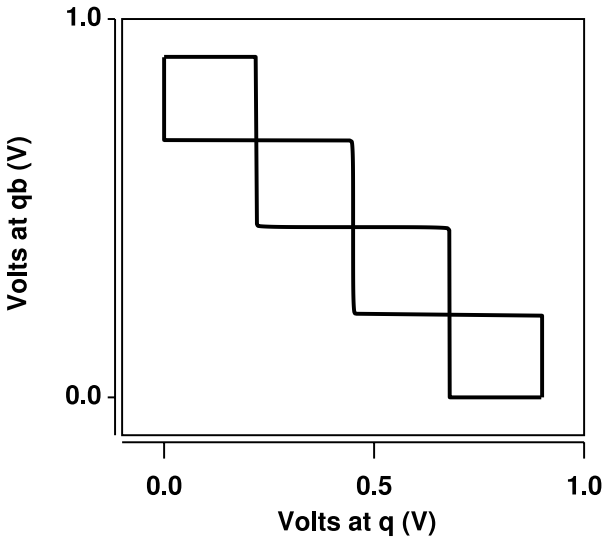


Fig. 15: The SNM of the proposed memory cells (butterfly diagram).

Tab. 9: Static noise margin of different design using butterfly diagram.

Design	SNM "0" (mV)	SNM "1" (mV)	SNM "2" (mV)	Cell SNM (mV)
[21]	310	150	310	150
[25]	300	160	300	160
[30]	285	300	285	285
Proposed	311	314	311	311

5. Discussion and Conclusion

In this paper, standard ternary logic gates are initially designed so that static power consumption and PDP drops sharply. With the assumption of having two source voltages, V_{DD} and $V_{DD}/2$, for generating logic '1', $V_{DD}/2$ source is directly switched to the output and all direct paths from sources to Ground are eliminated. Although using two supply voltages needs an excess line for $V_{DD}/2$, it causes a sharp reduction in static power if all direct current paths are removed. These gates can be used for low static power applications. Also, in this paper, a new low power memory

cell using the proposed STIs is designed. Simulation results, using HSPICE software and CNT 32 nm model, indicate that the proposed designs have lower power consumption and PDP compared to previous works.

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