Perspective of Buried Oxide Thickness Variation on Triple Metal-Gate (TMG) Recessed-S/D FD-SOI MOSFET

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Abstract. *Recently, Fully-Depleted Silicon on Insulator (FD-SOI) MOSFETs have been accepted as a favourable technology beyond nanometer nodes, and the technique of Recessed-Source/Drain (Re-S/D) has made it more immune in regards of various performance factors. However, the proper selection of Buried-Oxide (BOX) thickness is one of the major challenges in the design of FD-SOI based MOS devices in order to suppress the drain electric penetrations across the BOX interface efficiently. In this work, the effect of BOX thickness on the performance of TMG Re-S/D FD-SOI MOSFET has been presented at 60 nm gate length. The perspective of BOX thickness variation has been analysed on the basis of its surface potential profile and the extraction of the threshold voltage by performing two-dimensional numerical simulations. Moreover, to verify the short channel immunity, the impact of gate length scaling has also been discussed. It is found that the device attains two step-up potential profile with suppressed short channel effects. The outcomes reveal that the Drain Induced Barrier Lowering (DIBL) values are lower among conventional SOI MOSFETs. The device has been designed and simulated by using 2D numerical ATLAS Silvaco TCAD simulator.*

Keywords

Buried oxide, FD-SOI, Re-S/D, short channel effects.

1. Introduction

In current technological trends, high performance and low power devices are in demand for the faster operation of Integrated Circuits (ICs). However, the continuous scaling in MOS transistors beyond nanometer nodes affected the device performance. This results in various short channel effects, like Drain Induced Barrier Lowering (DIBL), Band-To-Band Tunnelling (BTBT), threshold voltage roll-off, subthreshold slope etc. [1], [2] and [3]. From past two decades, various technologies have been evaluated for the improvement in the device performance at such nodes. Mostly recommended technologies are fully-depleted silicon on insulator [4] and [5], FinFET [6], [7] and [8], tunnel field effect transistors [9].

Moreover, Buried Oxide based SOI MOS devices have gained popularity due to their control over higher drain electric field penetrations, lower parasitic junction capacitance, higher trans-conductance and controlled subthreshold swing [10]. SOI based substrates are also efficiently functional even in un-doped conditions; this made it a preferable choice among various device designers [11]. Moreover, FD-SOI is one of the popular un-doped MOS technology FD-SOI MOS structures exhibit excellent electrostatic characteristics and offer high performance for low power ICs [10]. FD-SOI technology also follows Moore's law [12]. The primary concern related to the FD-SOI based MOS devices is the selection of appropriate thickness and material of buried oxide layer [13]. So that, the device could efficiently conquer the electric field penetration at SOI/BOX interface at sufficient drain bias. Recently, the effect of back oxide thickness variation on the performance of FD-SOI MOSFET has also been discussed [14]. However, the problem associated with the FD-SOI structures is the higher series resistance [15] because of very thin layers of drain and source regions and that will result in lower drive current.

In order to solve this problem, Re-S/D FD SOI MOSFET has been evaluated [16]. In which, S/D re-

gions are extended deeper into the BOX layer. This modification resulted in higher drive current and enhanced immunity over short channel effects. The theoretical justifications regarding Re-S/D UTB FD-SOI MOSFET has been provided by proposing an analytical model for front and back gate [17].

Moreover, gate engineering techniques have also been emphasized in the past few years. As, Dual Metal Gate (DMG) technique offers better performance as compared to conventional structures [18] and [19]. Kumar et al. has discussed the various performance features of DMG FD-SOI MOSFET. The DMG technology offers a step-up potential profile that predominantly controls the threshold voltage roll-off in short channel MOSFETs due to different multi-gate work-functions. This has also been employed with the Re-S/D SOI MOSFETs for better results [19].

In continuation of the research, TMG technology has also been found as the prominent method to conquer the short channel effects and threshold voltage degradation. The incorporation of triple metal adds two step-up profile of potential distribution as compare to DMG [20]. The advantages of TMG have been discussed by the analytical model of surface potential [21]. Whereas, an analytical model for surrounding gate engineered TMG MOSFET has also been developed [22]. This incorporation effectively reduced the short channel effects in nanoscaled MOSFETs. TMG technology has also been adopted for the effective reduction of short dimension effects in Re-S/D FD-SOI MOSFETs.

Recently, the analytical model for the TMG Re-S/D FD SOI MOSFET has been deliberated at 90 nm gate length for the first time [23]. This paper correctly explains the two-step potential profile across the channel that assures the gate controllability over the device rather than drain. It is therefore necessary to evaluate the electrical performance over various design challenges of TMG Re-S/D FD-SOI MOSFET.

In this work, the effect of buried oxide thickness variation on the performance of Re-S/D FD SOI MOSFET has been presented. The primary objective of this work is to justify the electrical performance of the TMG Re-S/D FD-SOI MOSFET over various design challenges at nanometer nodes. The performance analysis of the studied device has been done on the basis of its surface potential profile and the threshold voltage at different BOX thickness. In order to verify the short channel immunity, the DIBL effects and subthreshold slope has also been taken under study. The impact of channel length variation has also been a part of the study for this work.

This paper has been organized as follows. Section 1. itself defines the introduction of recent reports related to the various device performance. The studied device structure and specifications are discussed in Sec. 2. The results of the numerical simulations are thoroughly discussed in Sec. 3. and conclusion is given in Sec. 4.

2. Device Structure and Specifications

The schematic of TMG Re-S/D FD SOI MOSFET has been shown in Fig. 1. The three metal gates of different work-functions (Φ_{m1}, Φ_{m2}, Φ_{m3}) have been used here with the length of L_1, L_2 and L_3. Here, the first metal gate is working as the control gate and second is as first screen gate. Third metal is the second screen gate which almost neglects the effects of drain electric field penetration towards the Si/BOX interface. The source and drain regions are highly doped, and low substrate doping has been taken here.

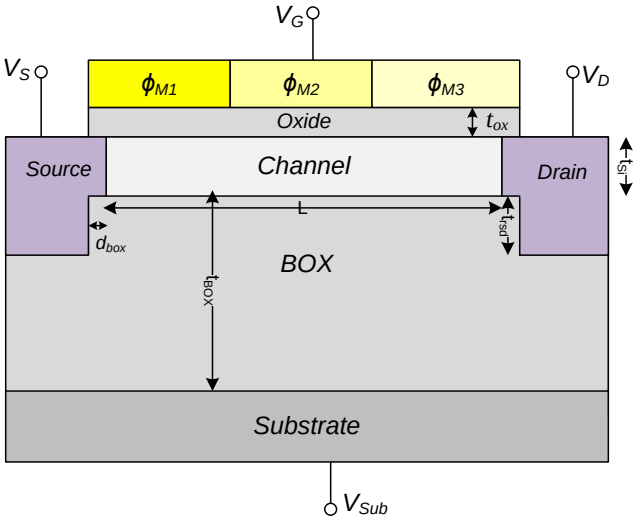

Fig. 1: Schematic of TMG Re-S/D FD SOI MOSFET.

Tab. 1: Various device parameters and their specifications.

Device parameters	TMG Re-S/D FD SOI MOSFET
Gate length	60 nm (variation: 30–70 nm)
Front oxide thickness (t_{ox})	2 nm
Doping density in Substrate regions	10^{15} cm^{-3}
Doping density in Source	Constant profile 10^{19} cm^{-3}
Doping density in Drain	10^{19} cm^{-3}
Back oxide (BOX) thickness (t_{BOX})	variation: 200–50 nm
Silicon Thickness (t_{Si})	10 nm
Device width	100 nm
t_{rsd}	30 nm
d_{box}	3 nm
Control Gate (Φ_{m1})	4.8 eV (Au)
First Screen Gate (Φ_{m2})	4.6 eV (Mo)
Second Screen Gate (Φ_{m3})	4.4 eV (Ti)

Table 1 shows the complete specifications of various device parameters. All the device parameters have been taken as per the ITRS guidelines. In Tab. 1, the variation of channel length and BOX thickness has been listed accordingly. The extension of drain and source regions in BOX layer has been written as t_{rsd} and the S/D overlap at the BOX layer as d_{box}.

2.1. Materials and Methodology Used

In this design, triple-metal-gate is used for analysis of BOX thickness variations. The main motive to use triple-metal gate engineering is to improve the device performance in terms of current drivability. As per earlier discussion, there are three regions in the gate-control gate, first screen gate and second screen gate. The work-function of the metal gate decreases by moving from the source side to drain side. Higher difference between source side work-function and drain side work-function increases the immunity to the variation of drain voltage which reduces DIBL. First gate, i.e. control gate requires high work-function material to increase the velocity of majority carriers, which increase the electric field across source side. Due to the increase of electric field the efficiency of current transportation is increased. So, Aurum (Au-gold) with the work-function of 4.8 eV is used. Screen gates have lower work-function to screen the source side with drain variation. In first screen gate, Molybdenum (Mo) with a work-function of 4.6 eV is used to make a first step-up potential profile. In the second screen gate, Titanium (Ti) with work-function of 4.4 eV is used to make second step-up potential profile.

3. Results and Discussion

The characterization of the TMG Re-S/D MOSFET has been done by 2D Silvaco ATLAS simulator. Different types of models are used to simulate the device such as CVT, SRH, CONMOB, FLDMOB, and Fermi [24]. CVT (Concentration Voltage Temperature) is concentration dependent mobility model which includes surface mobility degradation. SRH (Shockley Read-Hall) recombination model is used to calculate the lifetime of carriers. CONMOB (Concentration Dependent Mobility) model is a table to relate doping and field mobility. FLDMOB (Field Dependent Mobility) model is used to model velocity saturation effect. Fermi Dirac statistic model is used to reduce carrier concentration in heavily doped region.

Figure 2 shows the graph of surface potential at the interface of front and back channel. The minima of surface potential in the graph shows that the inversion is done at the interface of back channel before front channel interface. This indicates the significance and control over various leakages associated during off state. Form plot, the studied device successfully offers the three-step profile in surface potential at front channel interface due to inclusion of triple metal gate. This will screen-off the drain potential effects twice as compared to conventional dual metal gate structures and hence improved immunity to short channel effects.

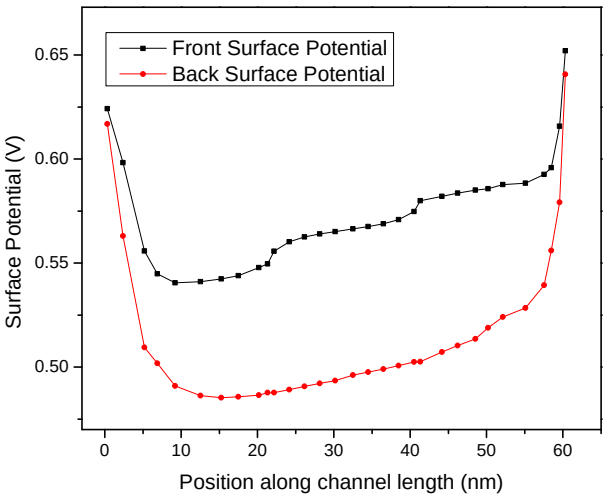

Fig. 2: Surface potential versus position of channel length at front and back channel interface.

The characteristic of the surface potential at front and back interfaces has been shown in Tab. 2. The surface potential minima position along the channel length has been observed near to the source side of the channel. This corresponds to more uniform electric field in the channel region and hence reduced short channel effects. Also, the back-channel potential is lower than the front potential. This signifies that the front surface potential is responsible for threshold voltage. So, for further verification, extraction of threshold voltage at different channel length and buried oxide thickness has been done.

Tab. 2: Characteristics of Surface Potential at 60 nm channel length.

Interfaces	Minima	Minimum surface potential
Front channel interface	$x = 9.21$ nm	0.54056 V
Back channel interface	$x = 15.24$ nm	0.48535 V

The graph of threshold voltage variation with channel length at the drain voltage of 0.05 V and 0.1 V has been drawn in Fig. 3. It shows the roll-off effect by varying drain voltage. One can observe from the plot that there is no roll off seen at higher drain voltages. This also justifies that the studied device is free form drain electric field penetrations and offers lower voltage of operation as well. Threshold voltage variation

with channel length at different buried oxide thickness for 0.1 V of drain bias is shown in Fig. 4. The threshold voltage is increased by decreasing BOX thickness which assures better immunity to short channel effect at small BOX thickness as compared to other reports [14]. Increasing BOX thickness reduces threshold voltage roll-off. So, there is less consumption of less fraction of gate voltage at thicker BOX layer.

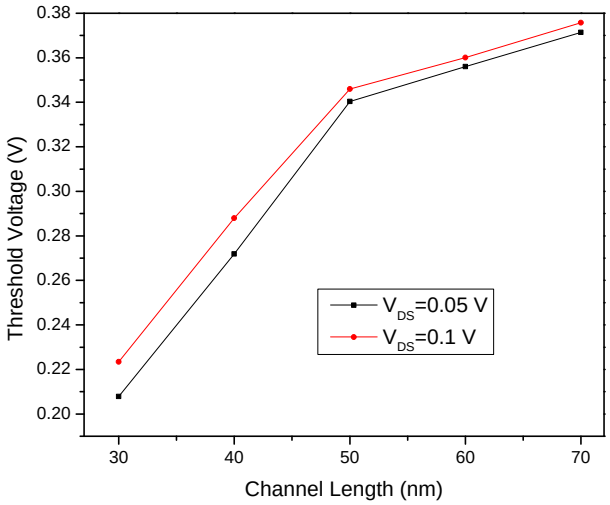

Fig. 3: Threshold voltage variation with channel length at different drain voltage.

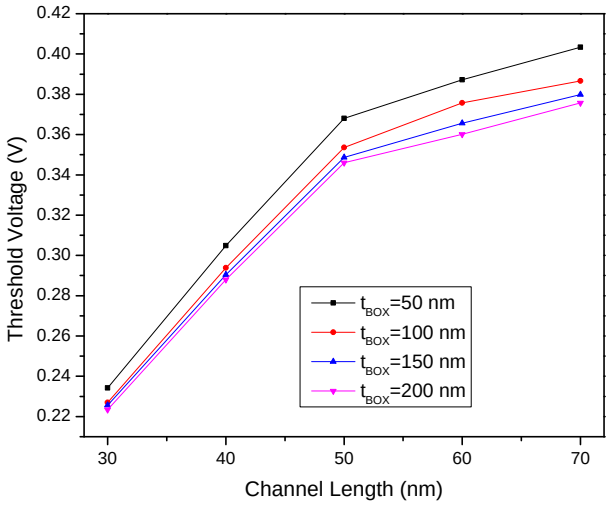

Fig. 4: Threshold voltage variation with channel length at different buried oxide thickness at $V_{DS} = 0.1$ V.

Figure 5 shows the graph of Drain Induced Barrier Lowering (DIBL) variation with channel length at different buried oxide thickness for $V_{DS} = 0.1$ V. It shows the less DIBL in the case of small BOX thickness which ensures better immunity to barrier lowering.

Figure 6 shows the sub-threshold slope variation with channel length at different BOX thickness for drain voltage of 0.1 V. It shows that subthreshold slope for the device moves towards ideal

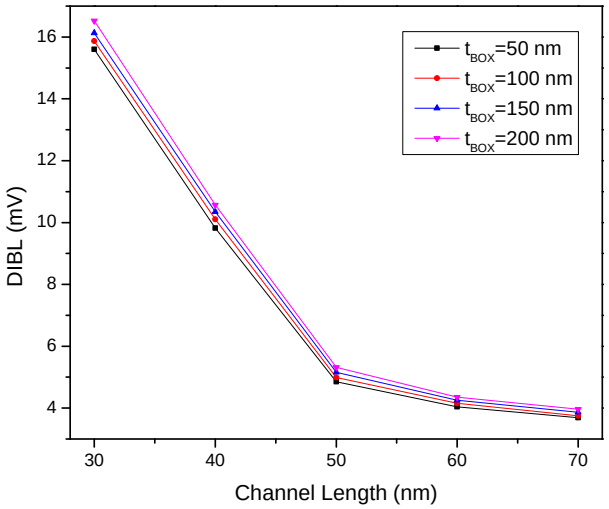

Fig. 5: DIBL variation with channel length at different buried oxide thickness at $V_{DS} = 0.1$ V.

value (60 mV·dec^{-1}) at small BOX thickness. It shows that sub-threshold slope is getting worse by decreasing channel length which indicates the slow transition between on and off state.

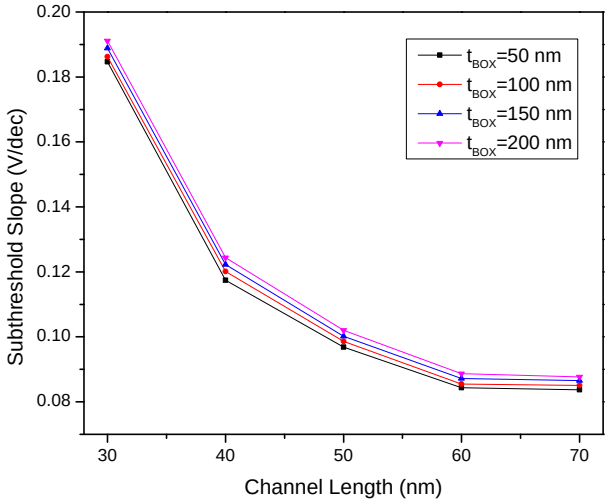

Fig. 6: Subthreshold slope variation with channel length at different buried oxide thickness at $V_{DS} = 0.1$ V.

From previous discussions, it has also been clarified that the device is free from small dimension effects at optimized buried oxide thickness and how the buried oxide is playing a significant role in the design of fully depleted SOI MOSFETs. For the exact analysis of current-voltage behavior, the input characteristics curve has been taken under study. The drain current vs. gate voltage plot for different BOX thickness for biasing of drain at 0.1 V is shown in Fig. 7. It can be seen from the figure that the device is showing almost negligible off-state leakage and offering better drive current. The I_{on}/I_{off} is calculated as $2.14 \cdot 10^9$ at BOX thickness of 50 nm.

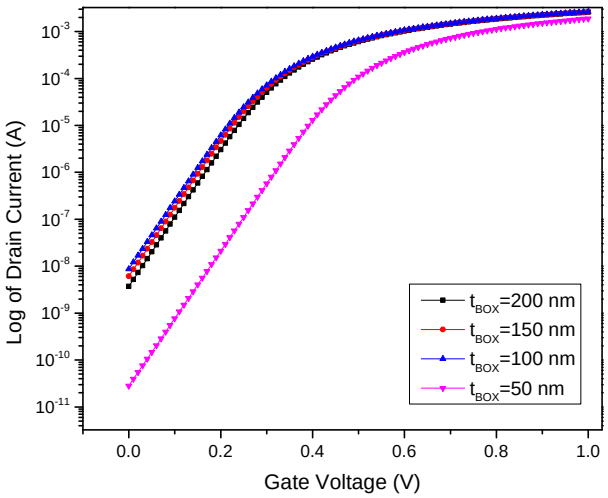

Fig. 7: The input characteristics curve (I_d vs V_{gs}) at different BOX thickness at $V_{DS} = 0.1$ V.

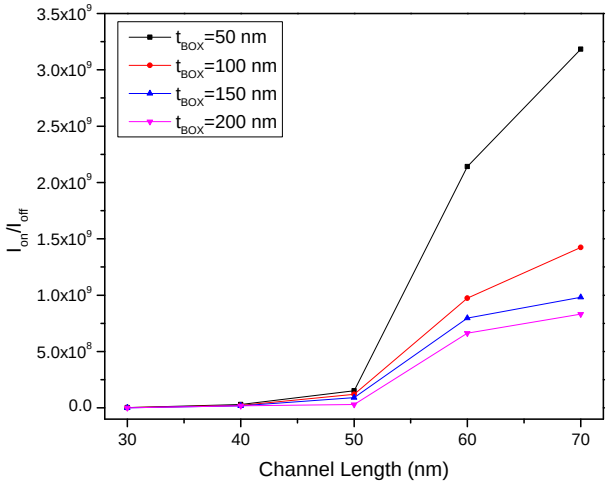

Fig. 8: Switching (I_{on}/I_{off}) current ratio variation with channel length at different buried oxide thickness at $V_{DS} = 0.1$ V.

Figure 8 shows the variation of on/off current ratio with channel length at different BOX thickness for $V_{DS} = 0.1$ V. The ratio of I_{on}/I_{off} is increased by decreasing BOX layer thickness which shows better on current at thinner BOX layer. It shows the better gate control at thinner BOX layer.

Further, for the study of analog performance of the device, transconductance analysis has been taken into account. The device transconductance with the variation in gate to source voltage at different BOX oxide thickness is shown in Fig. 9. The drain voltage is taken as 0.1 V. It is found from the plot that the value of transconductance is incrementing and it follows the pattern of drain current variation. However, at higher gate voltage levels, there is a significant drop recorded at all variations of BOX thickness and lesser at BOX of 50 nm. Moreover, it is seen from the plot

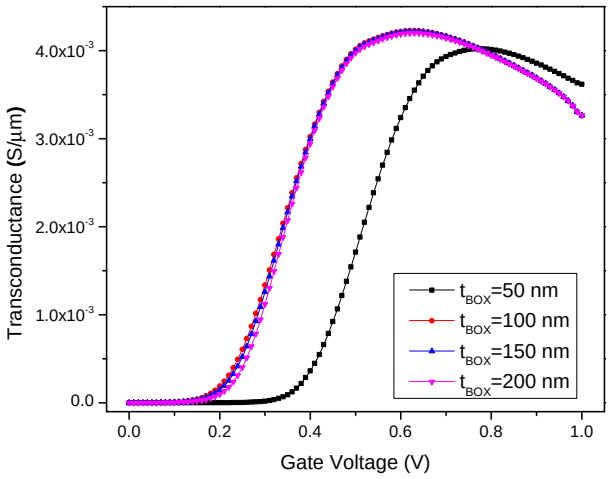

Fig. 9: Transconductance vs gate voltage plot with variation in buried oxide thickness at $V_{DS} = 0.1$ V.

that the transconductance value is also higher for the same BOX oxide thickness of 50 nm and calculated as $3.82 \cdot 10^{-9}$, which itself explains the analog performance of the studied device. This is due to the enhanced carrier transport efficiency of the TMG Re-S/D FD-SOI MOSFET. The various performance features at different BOX thickness have been listed in Tab. 3.

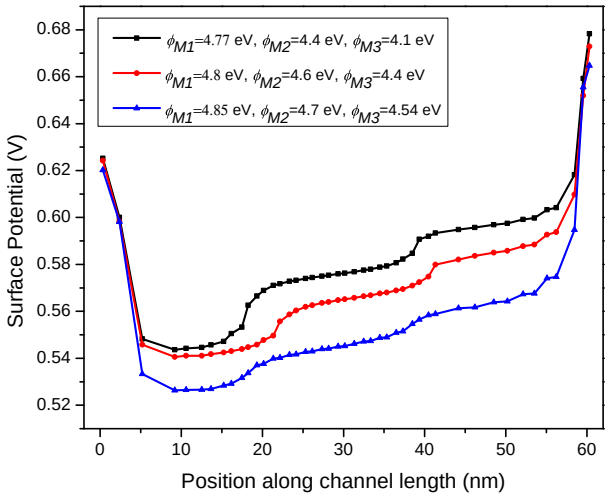

Fig. 10: Surface potential variation with the position along the channel for different work-functions of metal-gates at $V_{DS} = 0.1$ V.

The perspective of buried oxide thickness variation on triple metal-gate Re-S/D FD-SOI MOSFET can be clearly seen from Tab. 3. The optimized BOX oxide thickness is calculated as 50 nm. For further investigations, work-function engineering for these metal-gates has been taken into account at optimized BOX oxide thickness. Surface potential profile has been considered here for the work-function difference analysis. Figure 10 shows the plot of surface potential along the channel at different work-functions of metal

Tab. 3: Parameters value of the device for different BOX thickness at 60 nm channel length.

Parameters	$t_{BOX} = 50$ nm	$t_{BOX} = 100$ nm	$t_{BOX} = 150$ nm	$t_{BOX} = 200$ nm
Threshold (V)	0.38715	0.37575	0.3656	0.36009
DIBL (mV)	4.04	4.15	4.23	4.36
Subthreshold Slope (V·dec^{-1})	0.08433	0.08545	0.08717	0.08867
I_{on}/I_{off}	$2.14 \cdot 10^9$	$9.28 \cdot 10^8$	$7.96 \cdot 10^8$	$6.63 \cdot 10^8$
Transconductance (S·μm^{-1})	$3.82 \cdot 10^{-3}$	$3.26 \cdot 10^{-3}$	$3.26 \cdot 10^{-3}$	$3.27 \cdot 10^{-3}$

gates. It is clear from the plot that the control gate screening has been enhanced as the differences between the metal-gate work-functions are increased because of drain bias variations. Also, with the work-function engineering, the minima of the surface potential are getting changed. As, the work-function is decreased, the minima is shifting more along the source channel junction, which optimally controls the drain bias effects. However, the increment in the value of surface potential at this minima position along the channel leads to less immunity over short dimension effects. So, it is therefore necessary that one should trade-off as per the requirements.

4. Conclusion

In this paper, the performance evaluation of triple metal gate recessed source/drain FD SOI MOSFET has been done. The appropriate validations have been provided over various design challenges at nanometer nodes and it has been found that the studied device offers high performance and low power constraints. It has been verified that the device exhibits two step-up potential profile at the interfaces of metal gates and hence enhanced short channel immunity. It is also worth here to mention the threshold voltage results, as almost negligible roll-off has been observed at higher drain bias. From Tab. 3, the optimized buried oxide thickness has been calculated as 50 nm at 60 nm channel length and DIBL as 4.04 mV. The device is also offering higher drive current and low off-state leakage. The switching ratio (I_{on}/I_{off}) is found as 10^9, which is quite enough to stay over various off state leakage issues in the device. Hence, the studied device could be suggested as a future alternative for design of nanoscaled MOS integrated circuits.

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