Low Power Differential CMOS Schmitt Trigger with Adjustable Hysteresis

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Abstract. *This paper proposes a novel differential CMOS Schmitt trigger with adjustable hysteresis. The hysteresis of the proposed circuit is generated using cross-coupled pMOS or nMOS transistors, which can be tuned by engineering cross-coupled transistors current. By changing input voltage, the hysteresis window can also be adequately adjusted. Negative feedback has been introduced through CMOS differential amplifier which makes the circuit less sensitive to process, supply voltage and temperature (PVT) deviations. The proposed configuration uses TSMC 0.18 µm CMOS technology with 1.8 V supply voltage. Simulation results show that the switching voltage of the circuit can be tuned for target applications.*

Keywords

Adjustable hysteresis, low power, Schmitt trigger, self-biasing.

1. Introduction

A CMOS Differential Amplifier (CDA) is extensively used in analog and mixed-signal applications. CDA configuration is fully complementary and biased with negative feedback, which differs from the conventional CMOS differential amplifier. Moreover, CDA configuration comprises less die area, consumes less power and negative feedback that make the circuits less sensitive to Process, supply Voltage and Temperature (PVT) variations [1].

Schmitt trigger is a bistable circuit which is extensively used in both analog as well as digital signal processing systems to improve the circuit immunity against noise and disturbances [2] and [3]. The traditional Schmitt trigger is generally realised using operational amplifiers and resistors connected in positive feedback, which has the drawback of high-power consumption. Dokic [4] proposed three different designs of single-ended Schmitt trigger. In his two designs, three transistors are connected between power and ground rails while in third design, four transistors are connected between power and ground rails. This particular stacked design became a basic building block to prepare many complex Schmitt trigger circuits but is not preferable for the application where the supply voltage is low. Steyaert et al. [5] introduced a novel CMOS Schmitt trigger comprising of two inverters with an extra feedback transistor. Wang [6] proposed a low-power adjustable Schmitt trigger circuit. The most significant feature of this circuit is the hysteresis adjustment. Pfister [7] proposed a minor modification of [4] and converted it to the controllable hysteresis configuration. Kim et al. [8] introduced a new waveform-reshaping circuit which is considered as an alternative to the conventional Schmitt trigger. This configuration is suitable for high-speed system design because it uses the ratioless inverters, and these inverters do not require extra standby current. Al-Sarawi [9] proposed a Low power Schmitt trigger circuit which consists of six transistors set in a complementary MOS structure. Zhang et al. [10] presented CMOS Schmitt trigger circuits with the help of a substrate-bias technique which is suitable for low voltage applications. Pedroni [11] introduced an open-loop approach for designing a Schmitt trigger circuit which allows low voltage and high-speed operation compared to other traditional approaches. Vipul [12] proposed two new inverter-based designs, which are immune to kickback noise arise from the subsequent blocks. Sapawi et al. [13] presented

NAND gate based Schmitt Trigger design, which is suitable to operate for low voltage operation. Suresh [14] suggested modifications for Schmitt trigger circuit with self-bias transistor technique, which can operate for low power circuits. Meenali et. al. [15] presented Schmitt Trigger using body bias techniques to improve the timing and device leakage performance. Ke Lin et. al. [16] proposed PVT insensitive Schmitt trigger with fully adjustable hysteresis threshold voltages.

All the above-mentioned Schmitt Trigger circuits are single-ended configurations. Differential Schmitt trigger configuration developed from Allstot's design [17], [18] and [19] which is designed especially to use in wireless applications. Wei et al. [18] and [19] presented differential Schmitt trigger specifically designed for Asynchronous Sigma Delta Modulator(ASDM), which is further modified in [19] and [20] for programmable hysteresis. Yuan [2] and [3] introduced two new differential Schmitt trigger configurations with tunable hysteresis. The first configuration has used an inverter to generate hysteresis, while the second configuration has used regenerative current-feedback, which is suitable for low power and high-speed applications. Ali Nejati [20] proposed ultra-low voltage differential Schmitt trigger using bulk-driven and sub threshold techniques.

In this paper, three novel differential Schmitt trigger configurations are proposed. The proposed configurations of Schmitt trigger make use of the fully complementary CMOS differential amplifier. In the first design, self-biasing technique is used to avoid the separate biasing circuit for amplifiers while the second and the third design require separate biasing to adjust the hysteresis width of the circuit. However, all three configurations do not require individual amplifier biasing circuits, which save the total power and die area of the configuration. Rest of the paper is organized as follows: Sec. 2. provides brief description about differential CMOS Schmitt trigger proposed by Yuan [2]. Detail explanation of proposed low voltage differential CMOS Schmitt trigger is given in Sec. 3. Simulation results of the proposed Schmitt trigger designed in TSMC-0.18 µm using 1.8 V supply voltage are discussed in Sec. 4. Conclusion of the work is given in Sec. 5.

2. Differential CMOS Schmitt Trigger

Yuan [2] proposed Differential CMOS Schmitt trigger consisted of diodes connected in a differential pair with additional current sources as shown in Fig. 1. Hysteresis is introduced through two inverter circuits. For $V_{(IN+)} > V_{(IN-)}$, we first assume that the inverter feedback network (consists of M_7–M_{10} transistors) is

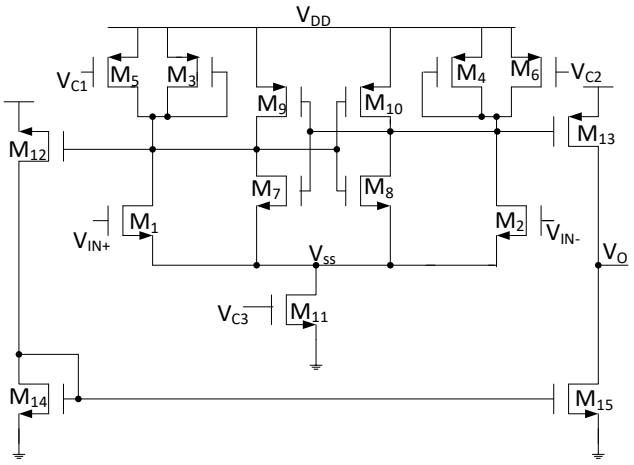


Fig. 1: Differential CMOS Schmitt trigger [2].

not activated then $V_{(IN+)} = (V_{SS} + V_T) + \sqrt{\frac{I_{D5}}{K_1}}$ and $V_{IN-} = (V_{SS} + V_T) + \sqrt{\frac{(I_{D6}}{K_2}}$. Here $K_{1,2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{1,2}$, V_T is the threshold voltage of MOS transistors, and V_{ss} is the voltage at node SS. Hence

$$V_{IN+} = V_{IN-} + \left(\sqrt{\frac{I_{D5}}{K_1}} - \sqrt{\frac{I_{D6}}{K_2}}\right). \tag{1}$$

When the inverter network is activated and $I_{D5} = K_1(V_{IN+} - V_{SS} - V_T)^2 + I_{D7}$ hence

$$V_{IN+} \approx \sqrt{\frac{I_{D5}}{K_1}}\left(1 - \frac{1}{2}\frac{I_{D7}}{I_{D5}}\right) + (V_{SS} + V_T). \tag{2}$$

Similarly, $K_2(V_{IN-} - V_{SS} - V_T)^2 = I_{D6} + I_{D10}$, therefore

$$V_{IN-} \approx \sqrt{\frac{I_{D6}}{K_2}}\left(1 + \frac{1}{2}\frac{I_{D10}}{I_{D6}}\right) + (V_{SS} + V_T). \tag{3}$$

By subtracting Eq. (3) from Eq. (2), V_{IN+} can be given by:

$$V_{IN+} = \left(V_{IN-} + \sqrt{\frac{I_{D5}}{K_1}} - \sqrt{\frac{I_{D6}}{K_2}}\right) - \frac{1}{2}\left(\frac{I_{D10}}{I_{D6}}\sqrt{\frac{I_{D6}}{K_2}} + \frac{I_{D7}}{I_{D5}}\sqrt{\frac{I_{D5}}{K_1}}\right). \tag{4}$$

By comparing Eq. (1) and Eq. (4), it is apparent that the second term in Eq. (4) measures the change of the switching voltage when the feedback network is initiated.

3. Proposed Low Voltage Differential CMOS Schmitt Trigger

In this section, three different CMOS differential amplifier based Schmitt trigger configurations are presented. In each circuit, additional transistors are connected in positive feedback, which introduces hysteresis in the circuit.

Figure 2 shows proposed Schmitt trigger schematic, which consists of two CMOS inverters (M_1–M_2 and M_3–M_4) and two transistors M_7 and M_8 which are biased in the triode region. The tail currents of the differential amplifiers become adaptive by connecting the gates of M_7 and M_8 to the drains of M_3 and M_4. PMOS transistors M_5 and M_6 add the hysteresis in the circuit. By keeping M_7 and M_8 transistors in the triode region, the proposed Schmitt trigger can deliver output switching currents that are significantly greater than its quiescent current. While in conventional CMOS differential amplifiers, switching currents can be limited by current-source [18], [19], [20] and [21]. This characteristic makes the proposed structure suitable for high-speed comparator applications.

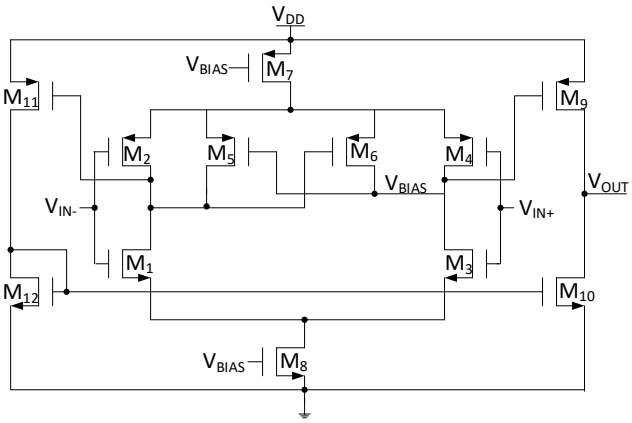


Fig. 2: Proposed Schmitt trigger schematic.

Considering the first case where hysteresis transistor M_6 is off, to make analysis simple, neglect the effect of channel length modulation. When $V_{IN-} < V_{IN+}$, the drains of M_1 and M_2 rise and turn off the M_6 transistor. At the same moment, M_3 and M_4 transistors remain in saturation. Saturation current is given as

$$I_{D3} = I_{D4}, \tag{5}$$

$$\frac{K_3}{2}\left(V_{IN+} - V_N - V_{Tn}\right)^2 = \frac{K_4}{2}\left(V_P - V_{IN+} - V_{Tp}\right)^2,$$

where $K_3 = \mu_3 C_{ox}\left(\frac{W}{L}\right)_3$, $K_4 = \mu_4 C_{ox}\left(\frac{W}{L}\right)_4$ and $V_T = V_{Tn} = |V_{Tp}|$.

If switching point of the inverter structure which consists of M_3 and M_4, is V_{TIN+}

$$V_{T_{IN+}} = \frac{V_P + V_T(R_1 - 1) + R_1 V_n}{R_1 - 1}, \tag{6}$$

where $R_1 = \sqrt{\frac{K_3}{K_4}}$, $K_3 = \mu_3 C_{ox}\left(\frac{W}{L}\right)_3$ and $K_4 = \mu_4 C_{ox}\left(\frac{W}{L}\right)_4$, V_n and V_p are the node voltages between M_3 and M_8 transistors and M_4 and M_7 transistors respectively.

In same manner:

$$V_{T_{IN-}} = \frac{V_P + V_T(R_2 - 1) + R_2 V_n}{R_2 + 1}, \tag{7}$$

where $R_2 = \sqrt{\frac{K_1}{K_2}}$ and $V_{T_{IN-}}$ is the switching point of the inverter structure consists of M_1 and M_2 transistors.

By subtracting Eq. (7) from Eq. (6) with assumption $R_1 = R_2$, i.e., if both the inverters are having perfect device matching then $V_{T_{IN-}} = V_{T_{IN+}}$. This shows that the switching of the circuit will occur when the input voltages become equal.

When M_6 transistor will be on, then positive feedback gets activated and current at the drain of M_3 and M_4 transistors would be:

$$I_{D3} = I_{D4} + I_{D6}, \tag{8}$$

$$\frac{K_3}{2}\left(V_{GS3} - V_T\right)^2 = I_{D4}\left[1 + \frac{I_{D6}}{I_{D4}}\right], \tag{9}$$

$$\sqrt{\frac{K_3}{2}}\left(V_{GS3} - V_T\right) = \sqrt{I_{D4}}\sqrt{1 + \frac{I_{D6}}{I_{D4}}}. \tag{10}$$

If the I_{D6} is small compared to I_{D4}, Eq. (10) can be simplified by formula given in [2].

$$\sqrt{1+x} \approx 1 + \frac{1}{2}x - \frac{1}{8}x^2 + \ldots \approx 1 + \frac{1}{2}x, \tag{11}$$

$$\begin{aligned}\sqrt{\frac{K_3}{2}}\left(V_{T_{IN+}} - V_n - V_T\right) = \\ = \sqrt{\frac{K_4}{2}}\left(V_P - V_{T_{IN+}} - V_T\right)\left(1 + \frac{1}{2}\frac{I_{D6}}{I_{D4}}\right),\end{aligned} \tag{12}$$

$$\begin{aligned}V_{T_{IN+}}\left(R + 1 + \frac{1}{2}\frac{I_{D6}}{I_{D4}}\right) = V_P + V_T(R-1) \\ RV_n + \frac{1}{2}\frac{I_{D6}}{I_{D4}}\left(V_P - V_T\right),\end{aligned} \tag{13}$$

where $R_1 = \sqrt{\frac{K_3}{K_4}}$ and $R_2 = \sqrt{\frac{K_1}{K_2}}$.

With perfect matching assumption, $R_1 = R_2 = R$.

In same manner,

$$I_{D1} = I_{D2} + I_{D5}, \tag{14}$$

$$V_{T_{IN-}}\left(R + 1 + \frac{1}{2}\frac{I_{D5}}{I_{D2}}\right) = V_P + V_T(R-1) + \\ + RV_n + \frac{1}{2}\frac{I_{D5}}{I_{D2}}(V_P - V_T). \tag{15}$$

By subtracting Eq. (13) from Eq. (15) and assuming $R+1+\frac{1}{2}\frac{I_{D6}}{I_{D4}}$ is almost same as $R+1$ and $R+1+\frac{1}{2}\frac{I_{D5}}{I_{D2}}$ is almost same as $R+1$:

$$V_{T_{IN-}} = V_{T_{IN+}} + \frac{V_P - V_T}{2(R+1)}\left[\frac{I_{D5}}{I_{D2}} - \frac{I_{D6}}{I_{D4}}\right]. \tag{16}$$

The change of the switching voltage can be quantified through Eq. (16). It is also observed that the hysteresis can be adjusted through changing the feedback current, I_{D6} and I_{D5}.

So by adding two transistors at the source of M_5 and M_6, the circuit can be converted into adjustable hysteresis configuration as shown in Fig. 3.

The positive feedback can also be generated using nMOS transistors in place of pMOS transistors, which suggests the possible modification to the structure shown in Fig. 3. The modified circuit with nMOS transistors is given in Fig. 4. Use of nMOS transistors will shift the hysteresis window without significantly affecting its width. This will help in applications where low die area is required.

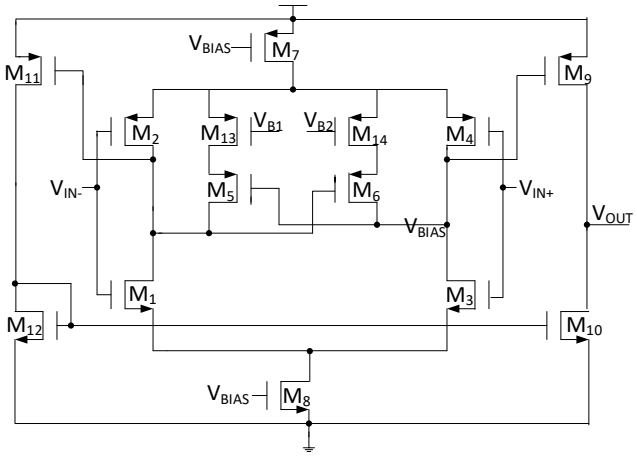


Fig. 3: Configuration for adjustable hysteresis with pMOS transistors.

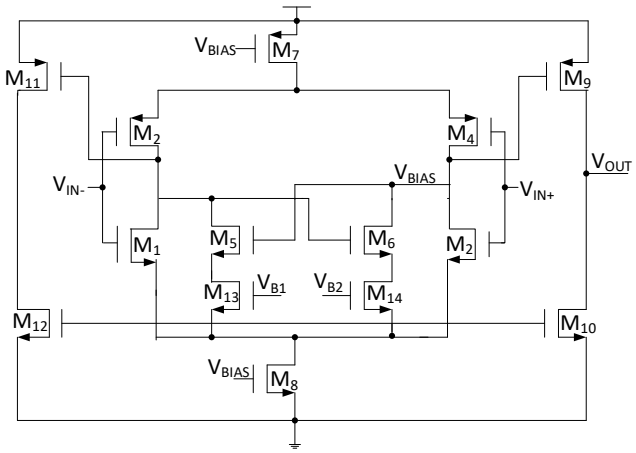


Fig. 4: Configuration for adjustable hysteresis with nMOS transistors.

4. Simulation Results

The Schmitt trigger circuits, shown in Fig. 2, Fig. 3 and Fig. 4 are designed and simulated using 0.18 µm CMOS technology in Cadence with 1.8 V supply voltage.

Figure 5 shows V_{OUT} when $V_{IN+} = 0.8$ V. It is noted that without the hysteresis transistor, the switching voltage of the proposed circuit is approximately 0.82 V. When the positive feedback is added with transistors M5 and M6 then circuit will observe hysteresis. Positive feedback also sharpens the state transition.

Figure 6 shows V_{OUT} with $V_{IN+} = 0.9$ V and $V_{IN+} = 1$ V. It is noted that the hysteresis window can be set by appropriate selection of V_{IN}. As discussed earlier that first proposed Schmitt trigger design, which is shown in Fig. 2, has used self-biased fully differential amplifier configuration, which is simulated through different PVT corners as per Tab. 1.

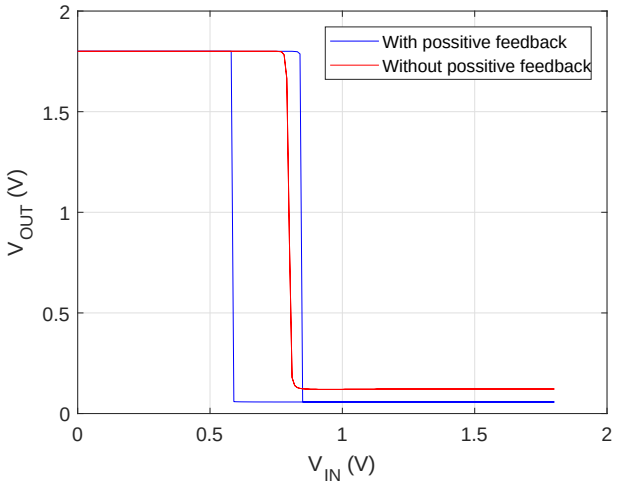


Fig. 5: DC Voltage Transfer characteristics for $V_{IN+} = 0.8$.

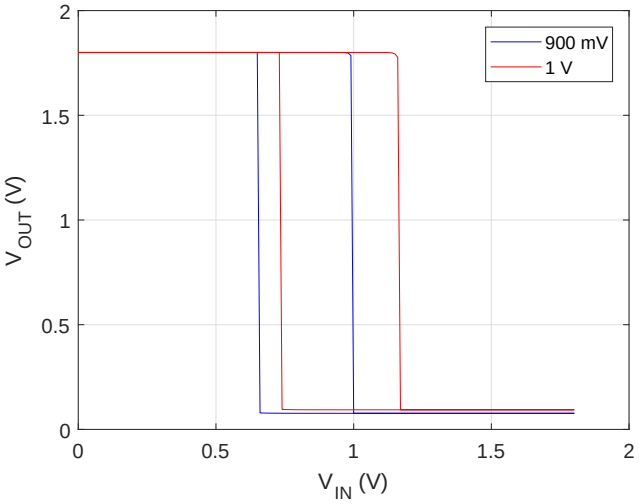
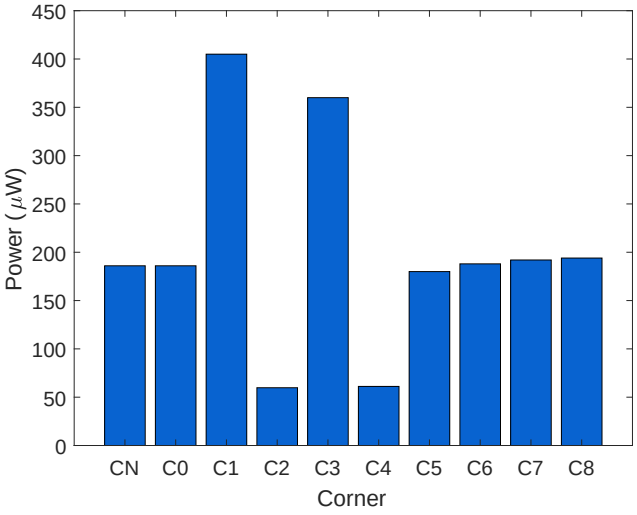


Fig. 6: DC voltage transfer characteristics for variation in V_{IN+} (Reference Voltage).

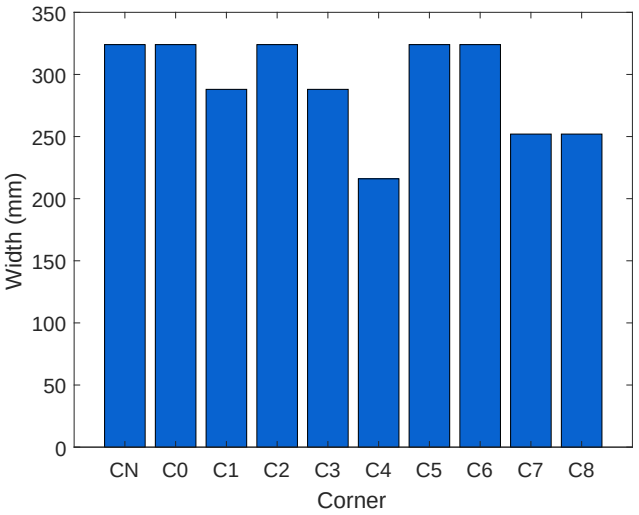


(b) Power.

Fig. 7: Schmitt trigger (represented in Fig. 2) for PVT Corners listed in Tab. 1.

The hysteresis width and power consumption for all the corners are depicted in Fig. 7(a) and Fig. 7(b). It can be noted that the hysteresis width varies less than ±0.072 V and variation in power consumption is very less for most of the corners. These results indicate that self-biasing concept will reduce the sensitivity of proposed Schmitt trigger to PVT variations, regarding hysteresis width and power consumption.

From Fig. 8, it is observed that the switching voltages and the hysteresis width of the circuit shown in Fig. 2, depend upon the positive feedback which specifically depends upon the feedback transistors (M_5 and M_6) width. It is noticed that the higher hysteresis width can be obtained with larger feedback current. Here V_{IN+} value set to 0.8 V and $W_{5,6}$ are varied from 500 nm to 900 nm with increments of 200 nm.



(a) Hysteresis width.

Tab. 1: List of PVT corners used in simulation.

Corner	Process	Supply Voltage (V)	Temperature (°C)
CN	Stat	1.8	27
C0	NN	1.8	27
C1	FF	1.8	27
C2	SS	1.8	27
C3	Stat	1.8	0
C4	Stat	1.8	40
C5	Stat	1.8	70
C6	Stat	1.8	100
C7	Stat	1.75	27
C8	Stat	1.85	27

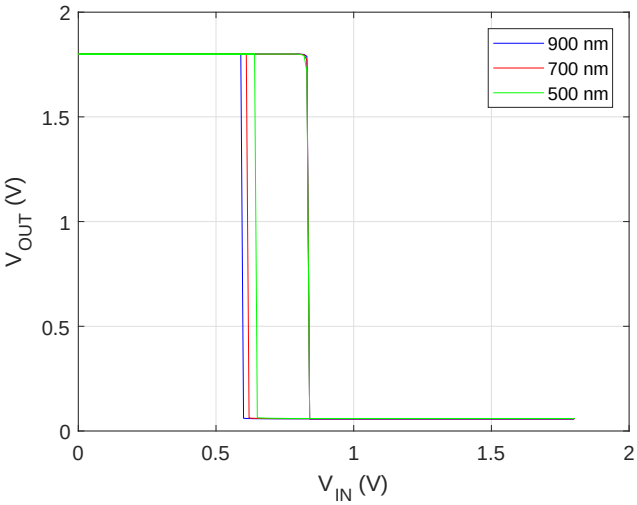


Fig. 8: Switching voltage dependence on feedback transistors (M_5 and M_6).

Figure 9 demonstrates that the hysteresis width of the proposed design shown in Fig. 3 depends on the bias voltages V_{B1} and V_{B2}. $V_{B1} = 0$ V and V_{B2} varies from 0.2 to 0.8 V with the step size of 0.2 V. It also

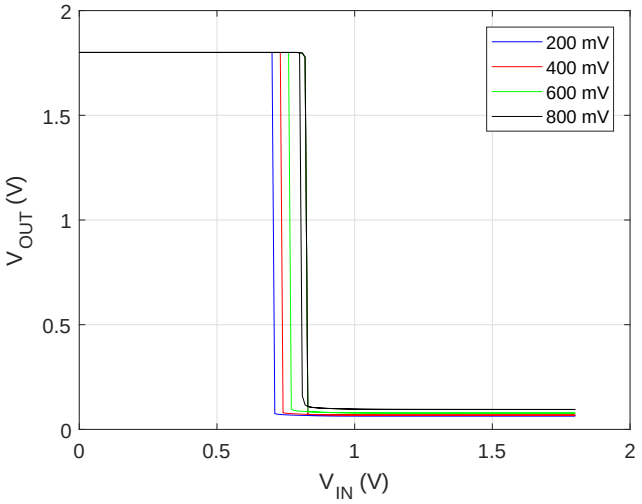


Fig. 9: Switching voltage dependence on control voltage V_{B2} when pMOS transistors used in positive feedback.

shows that by changing the V_{BIAS} voltage V_{B2}, the lower switching voltage and width of hysteresis can be adjusted.

Figure 10 shows the dependence of bias voltages V_{B1} and V_{B2} of nMOS transistors on the hysteresis width of the proposed configuration shown in Fig. 4. Here V_{B2} varies from 0.8 m to 1.4 V and $V_{B1} = 1.8$ V. By comparing Fig. 9 and Fig. 10 it can be concluded that due to the presence of nMOS transistors in feedback, lower threshold value remains fixed and hysteresis width can be tuned by changing the upper threshold voltage.

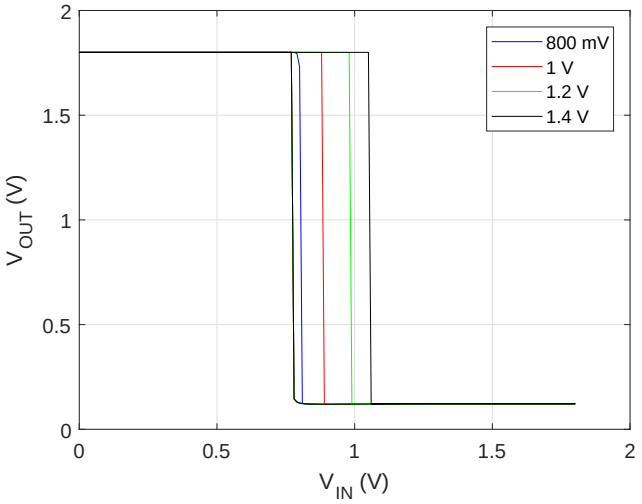


Fig. 10: Switching voltage dependence on bias voltage V_{B2} when nMOS transistors used in positive feedback.

Figure 11 shows the main application of the proposed Schmitt trigger. The input signal is the 50 MHz sine wave and output is the square wave. Schmitt trigger circuit can also be used to clean up the noisy signal. This can be explained through Fig. 12. The proposed circuit can be used as a quantizer for Asynchronous

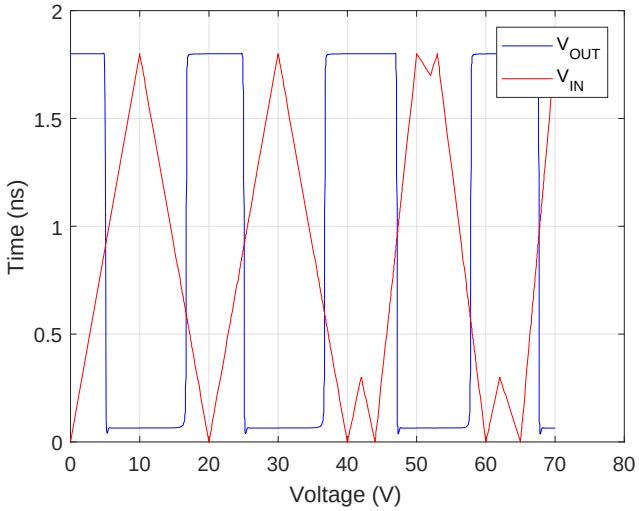


Fig. 11: Input ($V_{IN\text{-}}$) and Output (V_O) Waveform of Schmitt trigger indicates the sine to square wave conversation.

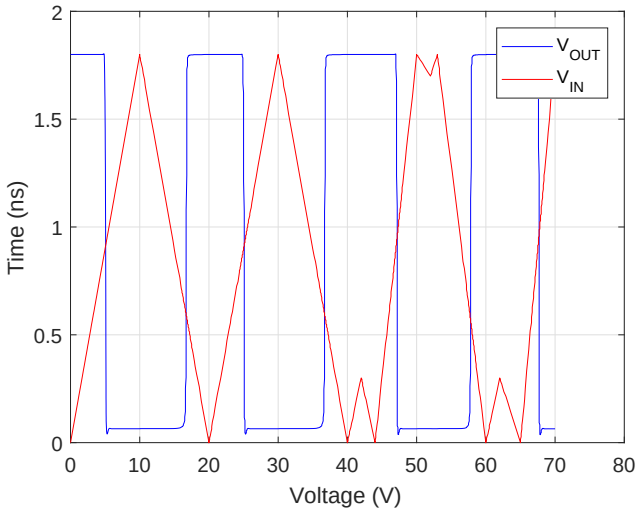


Fig. 12: Input ($V_{IN\text{-}}$) and Output (V_{OUT}) Waveform of Schmitt trigger. $V_{IN\text{-}}$ is a triangle waveform with voltage swing 0–1.8 V ($V_{IN+} = 0.8$ V).

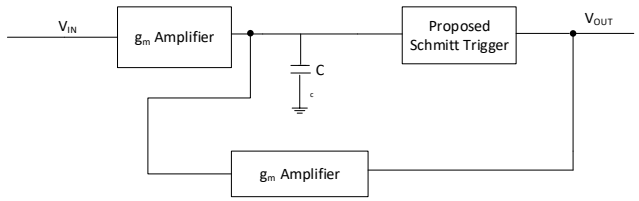


Fig. 13: Block diagram of Asynchronous Sigma Delta Modulator.

Sigma Delta Modulator (ASDM) (Fig. 13), where the input signal is applied to g_m–C integrator and then sent to the proposed Schmitt trigger. The waveform for the same is shown in Fig. 14.

From Fig. 15, it is observed that bias voltage (V_B) variation will create noteworthy change to the output

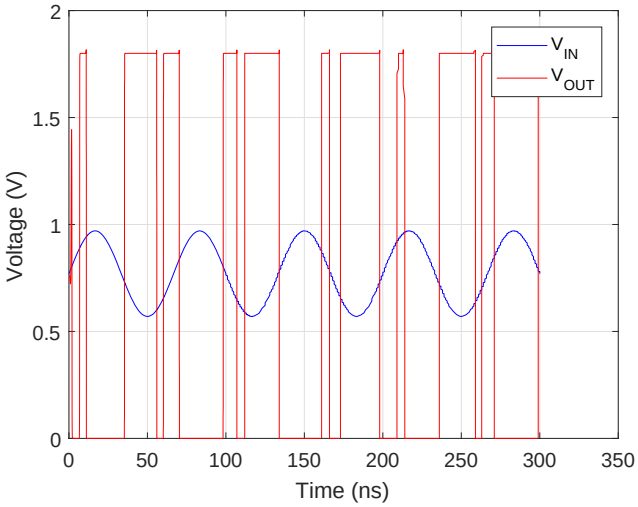


Fig. 14: Input and output waveform of ASDM.

current which will affect the total power consumption of the circuit.

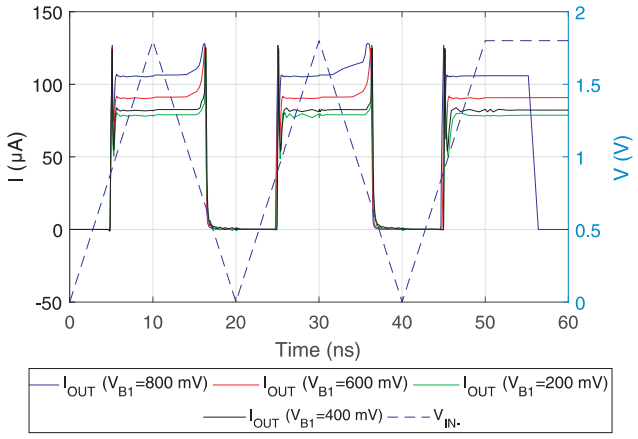


Fig. 15: Transient characteristic with variation in bias voltage.

Layout for the Proposed Schmitt trigger, represented in Fig. 3, is shown in Fig. 16. It is drawn using 0.18 μm technology and occupies an area of 24.1 μm × 28.1 μm.

Table 2 gives the comparison of existing Schmitt triggers with the proposed design. It shows that power consumption of the proposed Schmitt trigger circuit is quite low compared to existing differential Schmitt trigger design's simulation results, so it can be used in low power applications. The main advantages of the proposed circuit are differential configuration, variable hysteresis and fully complementary CMOS differential amplifier with no separate biasing require for amplifier, which makes it suitable for low voltage high-speed applications.

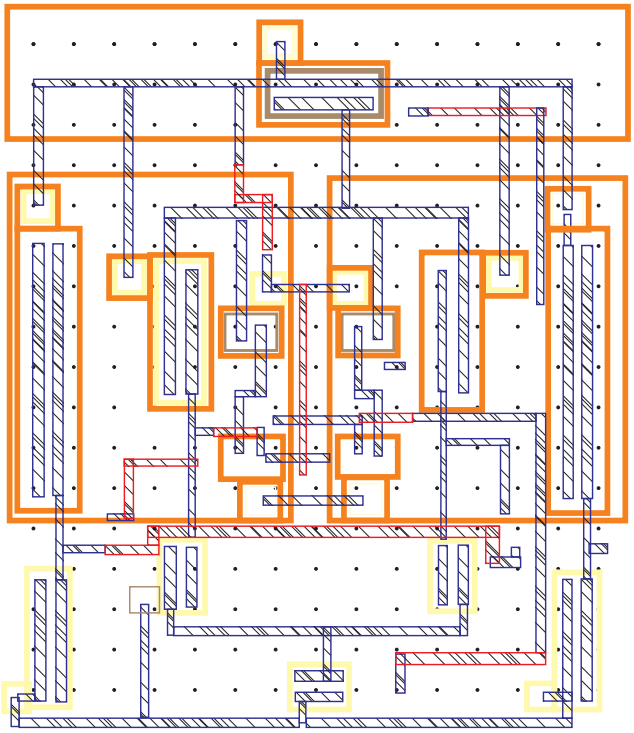


Fig. 16: Layout of proposed Schmitt trigger.

5. Conclusion

Three improved CMOS differential Schmitt trigger designs are proposed in this paper. The novel design approach uses a self-biasing techniques with fixed hysteresis width that makes the circuit less sensitive to PVT variations. In other two designs, additional transistors and biasing circuits, are added, which convert the circuits in tunable hysteresis. Also, it has been proved through simulation results that Hysteresis width can

Tab. 2: Comparison of existing Schmitt trigger circuits.

	Technology	Supply Voltage	Differential (D) Single Ended (S)	Fixed/Variable Hysteresis	Number of Transistors	Static Power Consumption
Proposed Design	180 nm	1.8 V	D	Variable	14	186 μW
Yuan [2]	180 nm	1.8 V	D	Variable	15+Bias	2.9 mW
Yuan [3]	180 nm	1.8 V	D	Variable	13+Bias	3.09 mW
Pingyun Wei [19]	0.6 μm	5 V	D	Variable	12+Bias	0.9 to 2.14 mW
Katyal [12]	180 nm	2 V	S	Fixed	8	NA
Suresh [14]	180 nm	0.8–1.5 V	S	Fixed	8	1.2 to 9.469 pW
Meenali Janveja [15]	180 nm	0.5 V	S	Fixed	8	2.52 μW
Ke Lin [16]	130 nm	1 V	S	Variable	28	2.51 μW

be controlled by varying biasing voltage. Proposed circuits can also be used as comparator by adjusting the control voltage across the feedback transistors. Despite simple configuration, the proposed Schmitt trigger is useful for applications where power and area requirements are less.

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