SIMULATION OF ELECTRICAL PARAMETERS FOR Ru/Ta_2O_5/SiO_2/Si(p) HIGH - κ MOS STRUCTURE

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Summary The contribution presents the results of simulation of direct tunnelling of free charge carriers through a thin gate insulator in MOS structures consisting of a Ta_2O_5/SiO_2 bilayer taking into account also indirect tunnelling of free charge carriers through the SiO_2/Si interface traps. The calculated *I–V* and *C–V* curves reveal the processes of electron and hole tunnelling through the insulator-to-semiconductor potential barrier that can be divided into four classes.

1. INTRODUCTION

MOS structures with a thin high-κ oxide layer and a metallic gate represent a new generation of unipolar integrated circuits [1, 2]. Analysis of the physical phenomena in the MOS structure requires a deep knowledge of the kinetics of processes taking place in the oxide layer and in the working region of the semiconductor. Simulation of these phenomena is a contribution to the solution of the capacitance and current properties of the MOS structure with thin high- κ oxide gate oxide layers.

The physical model of the MOS structure is based on our experience with simulating the properties of Schottky structures. By enhancing the thermionic emission-diffusion theory derived for metal-semiconductor barriers by Crowel and Sze [3] we have managed to develop the tunnelling-diffusion theory applicable to high-κ structures. The asset of this paper is an improved model that accounts also for the effect of the traps at the SiO_2/Si interface.

2. THEORY

The total electron and hole current flowing through the high-κ MOS structure as expressed by the tunnelling-diffusion theory is given by Eqn. (1).

Single current components are schematically shown in Fig. 1.

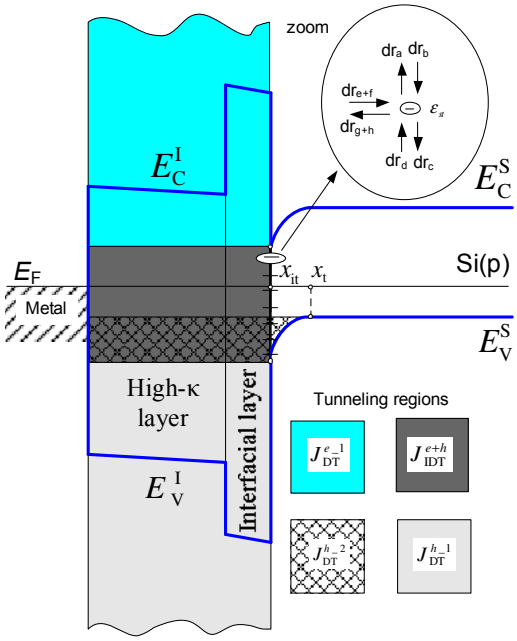

Fig. 1 Band diagram of a MOS structure showing the boundaries for calculation of tunnelling currents.

$$J^{e,h} = \mu q \frac{\left(v_{R\,DT}^{e,h} + v_{R\,IDT}^{e,h}\right) v_D^{e,h}}{v_{R\,DT}^{e,h} + v_{R\,IDT}^{e,h} + v_D^{e,h}} \left[v_{S0}^{e,h} \left(\exp\left(\pm \frac{q V_a^S}{kT} \right) - \frac{v_{GDT}^{e,h} + v_{GIDT}^{e,h}}{v_{R\,DT}^{e,h} + v_{R\,IDT}^{e,h}} \right) + \frac{J_{R\,DT}^{e,h\_2}(x_{it}) - J_{GDT}^{e,h\_2}(x_{it})}{q\left(v_{R\,DT}^{e,h} + v_{R\,IDT}^{e,h}\right)} + v_{T\_RG}^{e,h} \right] \qquad (1)$$

This formula considers direct tunnelling of free charge carriers through the oxide layer as well as indirect tunnelling via interface traps in terms of the velocities of direct and indirect tunnelling, $v_{G,R\,DT}^{e,h}$ and $v_{G,R\,IDT}^{e,h}$, respectively, and the drift-diffusion mechanism expressed by corresponding velocity, $v_D^{e,h}$.

2.1 Direct Tunnelling (DT)

The velocities of direct tunnelling of electrons and holes are given by [4]

$$v_{R\,DT}^{e,h} = \frac{J_{R\,DT}^{e,h\_1}}{q\,v_S^{e,h}} \qquad (2)$$

$$v_{\mathrm{G\,DT}}^{e,h} = \frac{J_{G\,DT}^{e,h\_1}}{q\,\upsilon_{\mathrm{S0}}^{e,h}} \qquad (3)$$

where the lower indices RDT and GDT are abbreviations for the apparent recombination and generation velocities of free charge carriers due to direct tunnelling. The electron tunnelling currents through the insulator, $J_{\mathrm{R,G\,DT}}^{e,h\_1}$, and the tunnelling currents through the insulator-semiconductor interface, $J_{\mathrm{R,G\,DT}}^{e,h\_2}(x)$, are computed from integrals

$$J_{\mathrm{G,RDT}}^{e,h\_1,2}(x_{it},x) = \int_{E_{C,V}^{S,I}(x_{it}),E_{C,V}^{S}(x_t)}^{E_{C,V}^{I,S}(x_{it}),E_{C,V}^{S}(x)} \int_0^{\infty} \frac{\mathrm{d}E_{\parallel}\,\mathrm{d}E_{\perp}}{1+\exp\left(\dfrac{\pm\left(E_{\parallel}+E_{\perp}\right)\mu\,E_{F,}E_F^{e,h}}{kT}\right)} \frac{q\,m_e^*}{2\pi^2\eta^3}\,\Gamma^{e,h}\left(E_{\perp}\right) \left\{\frac{\exp\left(\dfrac{\pm\left(E_{\parallel}+E_{\perp}\right)\mu\,E_F^{e,h},E_F}{kT}\right)}{1+\exp\left(\dfrac{\pm\left(E_{\parallel}+E_{\perp}\right)\mu\,E_F^{e,h},E_F}{kT}\right)}\right\} \qquad (4)$$

In these formulae the total energy of free charge carriers, E, is expressed as a sum of its two components: parallel and perpendicular to the surface, $E_{\parallel}$ and $E_{\perp}$. $\Gamma^{e,h}$ are tunnelling transmission coefficients, E_F is the Fermi energy in the metal that is taken to be a reference, and $E_F^e(x)$, $E_F^h(x)$ are electron and hole quasi-levels in the semiconductor.

2.2 Drift-Diffusion (D)

Symbol $v_D^{e,h}$ in Eqn. (1) stands for the velocity of electron and hole diffusion defined as

$$\frac{1}{v_D^{e,h}} = \int_{x_{it}}^{x_t} \frac{q}{kT\mu^{e,h}(x)} \exp\left(\mu\,\frac{\psi^{e,h}(x)-\psi^{e,h}(x_{it})}{kT/q}\right)dx \qquad (5)$$

Here, $\psi^{e,h}$ is the electric potential in the MOS structure.

2.3 Tunnelling and Recombination-Generation (T_RG)

Symbol $\upsilon_{T-RG}^{e,h}$ in Eqn. (1) denotes a quantity having a dimension of concentration defined as

$$\upsilon_{\mathrm{T\_RG}}^{e,h} = \int_{x_{it}}^{x_t} \frac{\left\{J_{\mathrm{R\,DT}}^{e,h\_2}(x) - J_{\mathrm{G\,DT}}^{e,h\_2}(x) + q\int_{x_{\mathrm{int}}}^{x}(R-G)dx'\right\}}{kT\mu^{e,h}(x)} \exp\left(\mu\,\frac{\psi^{e,h}(x)-\psi^{e,h}(x_{it})}{kT/q}\right)dx \qquad (6)$$

This term takes into account all mechanisms of bulk generation and recombination that contribute to the charge transfer in the semiconductor. These include also direct electron and hole tunnelling through the insulator into the bulk of the semiconductor, $J_{\mathrm{G\,DT}}^{e,h\_2}(x)$, and in the opposite direction, $J_{\mathrm{R\,DT}}^{e,h\_2}(x)$.

2.4 Indirect Tunnelling (IDT)

The theory of indirect tunnelling considers tunnelling of free charge carriers from the metal throught the insulating layer onto interface traps. In our model, indirect tunnelling is taken into account by means of generation and recombination velocities of indirect tunnelling. Details are given in the paper to appear in [5].

3. SIMULATION

3.1 Simulations of Ru/Ta_2O_5/SiO_2/Si(p)

In our simulations we considered a MOS structure with a layer of Ta_2O_5 and a thin intermediate layer of SiO_2, which is typical for structures containing a high-κ layer deposited on an p-type silicon substrate with acceptor concentration about 10^{21} m^{-3}. Material parameters of the substrate and of the oxide layers used in the simulations of *I–V* and *C–V* curves are shown in the band diagram in Fig. 2. In Eqn. (4) we considered effective electron and hole masses for silicon, thus $m_e^* = 2.1\,m_0$ and $m_h^* = 0.66\,m_0$. The tunnelling coefficients $\Gamma^{e,h}$ were calculated using the WKB method [6] for MOS structures. In the simulations we examined how the *I–V* and *C–V* curves changed with a varying thickness of the insulating layer. At first we considered a Schottky structure without an insulating layer. Then we simulated a MOS structure containing only a SiO_2 insulating layer with a thickness of 1.8 nm. Eventually, to a 1.8 nm thick layer of SiO_2 we added a layer of Ta_2O_5, varying its thickness from 0.2 to 18.2 nm. Simulations of *I–V* characteristics were performed using the models considering only direct tunnelling and also indirect tunnelling through surface traps. The simulated *I–V* curves clearly reveal the effect of indirect tunnelling upon the currents.

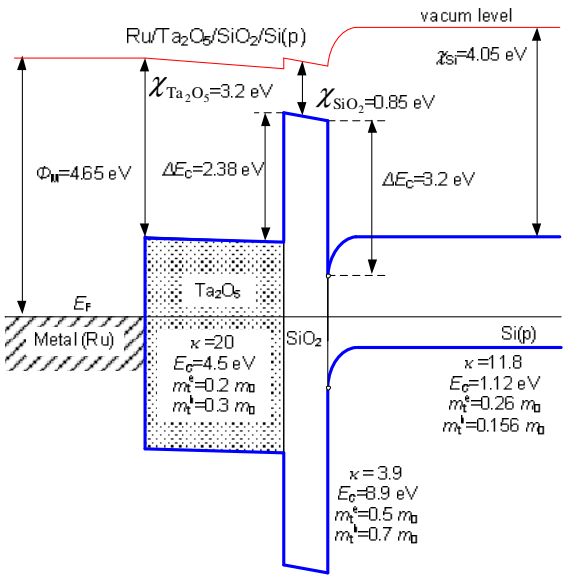

Fig. 2 Band diagram of a Ru/Ta₂O₅/SiO₂/Si(p) MOS structure with material parameters.

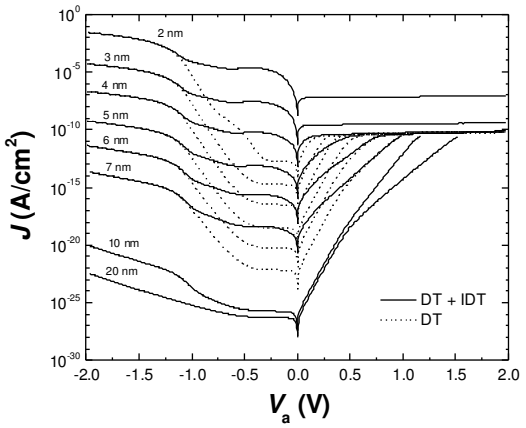

Fig. 3 Current densities through Ru/Ta₂O₅/SiO₂/Si(p) structure for various thicknesses of the oxide layer.

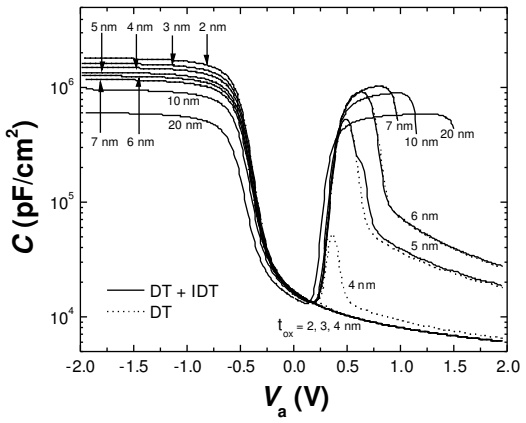

Fig. 4 Capacitance curves of the Ru/Ta₂O₅/SiO₂/Si(p) structure for variable thickness of the oxide layer.

The effect of indirect tunnelling is particularly important at low voltages. Due to indirect tunnelling, the currents are higher by 4 to 5 orders of magnitude than in the case that only direct tunnelling is considered. In a reverse biased structure (mode of inversion) the effect of space charge limited current is observed. This phenomenon is caused by the fact that the tunnelling probability of electrons is much higher than that of the holes. This is why virtually the whole current flowing through structures with $t_{OX} > 4$ nm has only an electron component. With an increase of $V_a \propto V_a^S > 0$ (inversion), the diffusion velocity of electrons is $v_D^e << \left(v_{RDT}^e + v_{RIDT}^e\right)$ or and it falls down exponentially with the applied voltage. Then, the electron current in this mode is limited by the value $J^e \cong q v_D^e \upsilon_{S0}^e \exp\left(qV_a^S / kT\right)$ that practically does not change because the exponential term is compensated by the diffusion velocity $v_D^e \propto \exp\left(-qV_a^S / kT\right)$. For $t_{OX} < 4$ nm also the hole component begins to play its role. It is limited in the whole range of voltages by direct and indirect tunnelling because $v_D^h >> \left(v_{RDT}^h + v_{RIDT}^h\right)$. For $t_{OX} \Rightarrow 0$ the MOS structure changes into a Schottky structure in which majority carriers dominate the charge transport.

In a forward bias MOS structure, a region of negative dynamic resistance is observed on the *I–V* curves. The model of indirect tunnelling allows to elucidate this phenomenon. Simulations reveal that this effect cannot be caused by sole direct tunnelling. In the region of the negative resistance the whole current is given by the hole constituent J_{IDT}^h that can be approximated by formula $J_{IDT}^h \cong q v_{RIDT}^h \upsilon_{S0}^h \exp\left(-qV_a^S / kT\right)$. The hole current follows the product $v_{RIDT}^h \exp\left(-qV_a^S / kT\right)$ because $q\upsilon_{S0}^h$ is constant. In the range between –0.4 to –0.6 V the product slightly decreases giving rise to the negative resistance.

Figure 4 shows simulated *C–V* curves of the Ta_2O_5/SiO_2 structure. In inversion, the minority carriers (electrons) saturate at lower concentrations for thinner insulating layers. This fact is enhanced by the mechanism of indirect tunnelling. The structures with thin oxide layers behave similarly like Schottky structures. The onset of inversion is blocked by tunnelling.

The *C–V* curve of the MOS structure is calculated from the common formula

$$C = C_{ox}\, C_S / \left(C_{ox} + C_S\right), \qquad (7)$$

where C_{ox} is the total capacitance of the sandwich oxide layer. In a real case it might be composed of several oxide layer, thus

$$C_{\mathrm{ox}} = \left(\sum_{i=1}^{N} t_{\mathrm{ox}_i} / \varepsilon_0 \kappa_i \right)^{-1} \qquad (8)$$

and C_S is the differential capacitance of the semiconductor

$$C_S = \mathrm{d}\left(Q_f + Q_{SC}\right) / \mathrm{d}V_a^S . \qquad (9)$$

Here, Q_{SC} is the total integral charge in the semiconductor

$$Q_{SC} = q \int_{x_{it}}^{w} \left(p - n + N_D - N_A\right) \mathrm{d}x \qquad (10)$$

and Q_f is the fixed interface charge.

With the onset of inversion one can observe a rise in the capacitance which, however, dos not saturate as it is the case of MOS structures with thick oxide layers but culminates and begins to fall down again with a further increase of the applied negative voltage. A further increase of the negative applied voltage brings about a decrease in capacitance. The growth of Q_{SC} stagnates because the concentration of minority carriers at the interface does not grow with the applied voltage.

4. CONCLUSION

The enhanced model of the transport of free charge carriers through the potential barrier of the insulating layer in MOS structures taking into account the effect of insulator-to-semiconductor interface traps provide a good insight into the kinetics of the MOS structure. Analysis of experimental data by means of simulations allows to define more accurately the electrophysical parameters of the MOS structure, first of all the amount and electric activity of the interface traps.

The calculated *C–V* curves of the $Ru/Ta_2O_5/SiO_2/Si(p)$ structure show a strong decrease of capacitance in inversion for oxide bilayers below 4 nm in thickness. In *I–V* curves, the negative dynamic resistance is typical in accumulation, which confirms the dominance of the flow of free charge carriers via the $SiO_2/Si(p)$ interface.

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